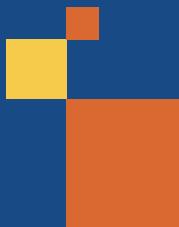


# Intel® Network Builders Insights Series

## Intel IPUs Fundamental Role In Your Cloud Strategy

- Xiaojun (Shawn) Li, Sales Director, Next Wave OEM & eODM
- Brian Niepoky, Director Connectivity Group Marketing
- Sabrina Gomez, Director Programmable Solutions Group Marketing

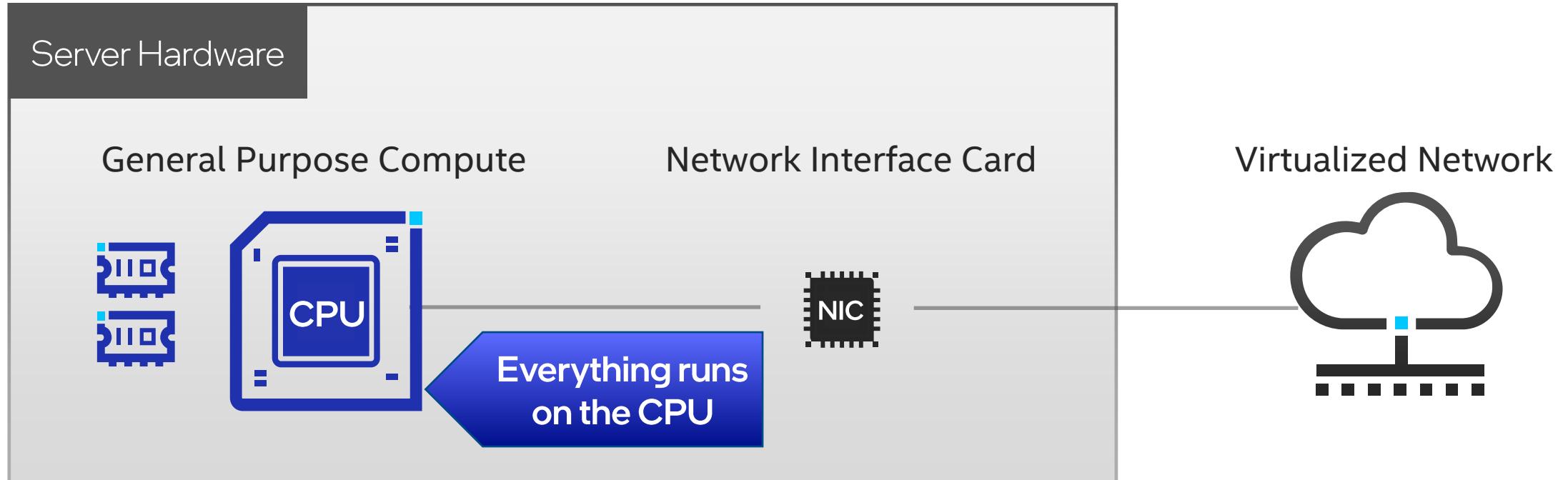


# Notices and Disclaimers

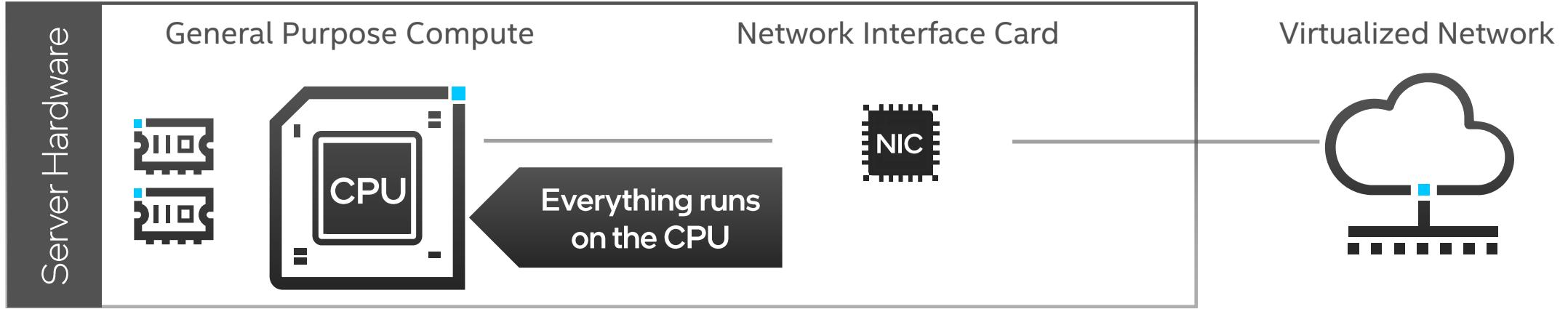
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- Your costs and results may vary.
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# Server Architecture in a classic Data Center

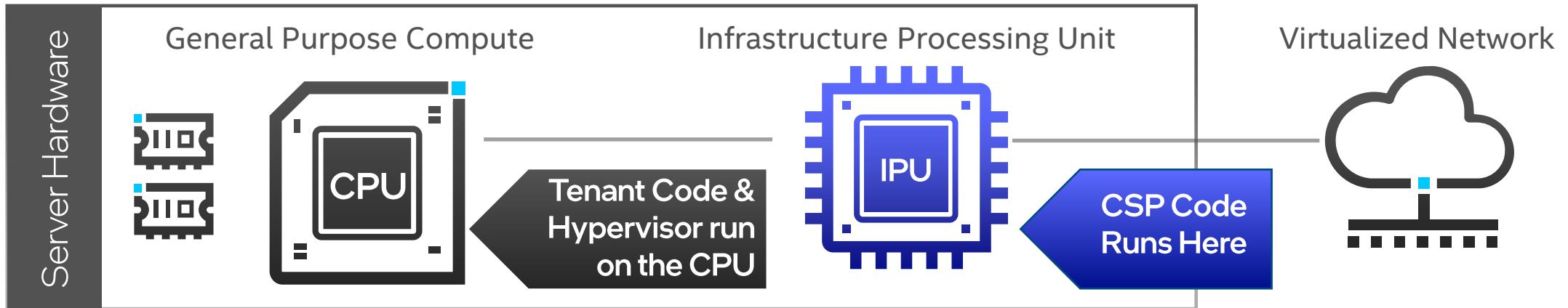
Software and Infrastructure are all controlled by One Entity

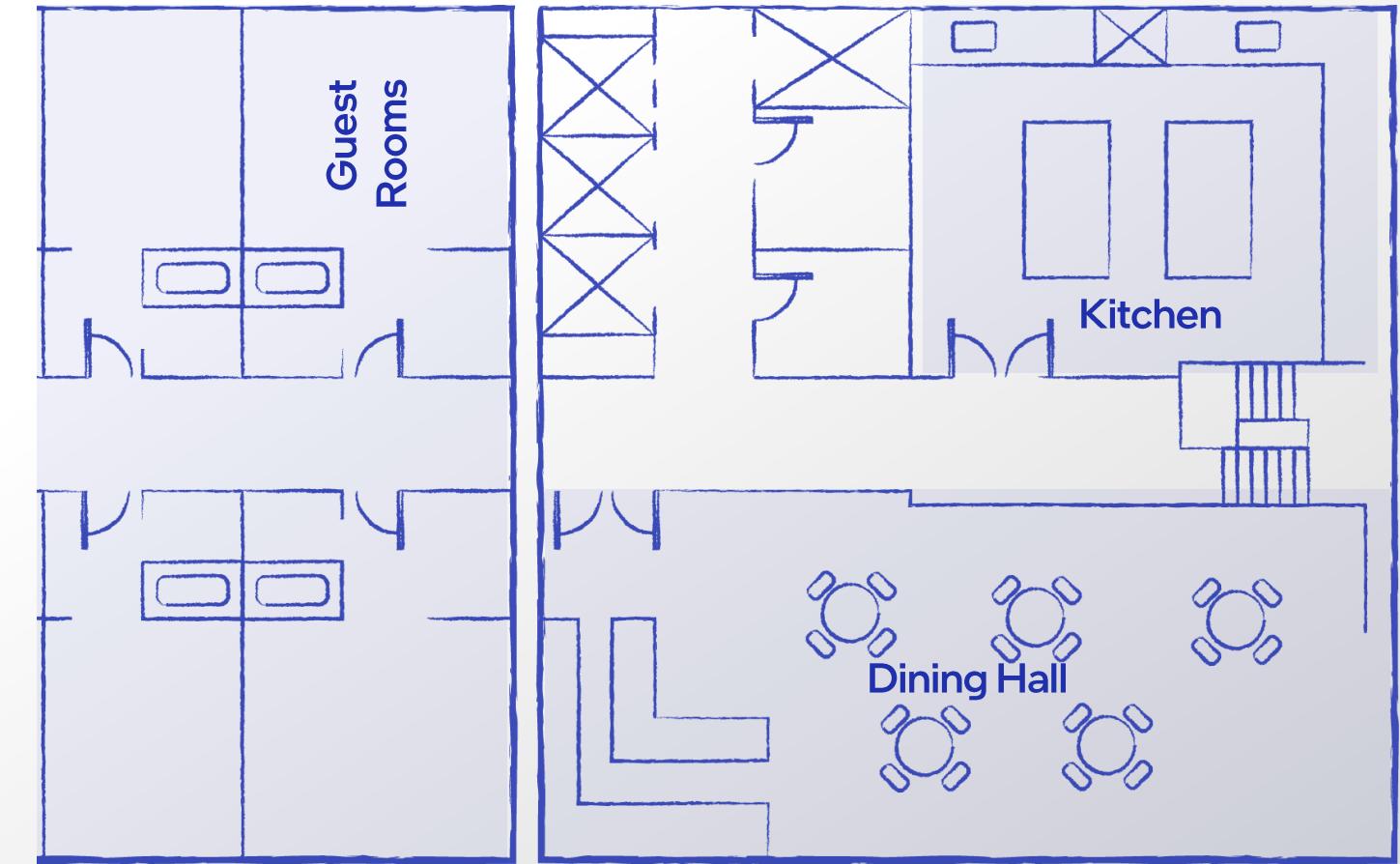
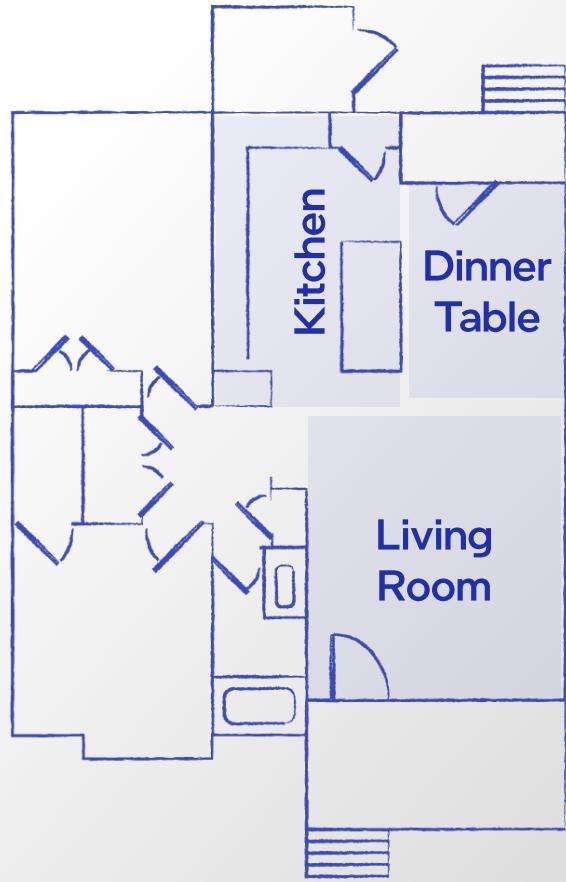


# Classic Server Architecture



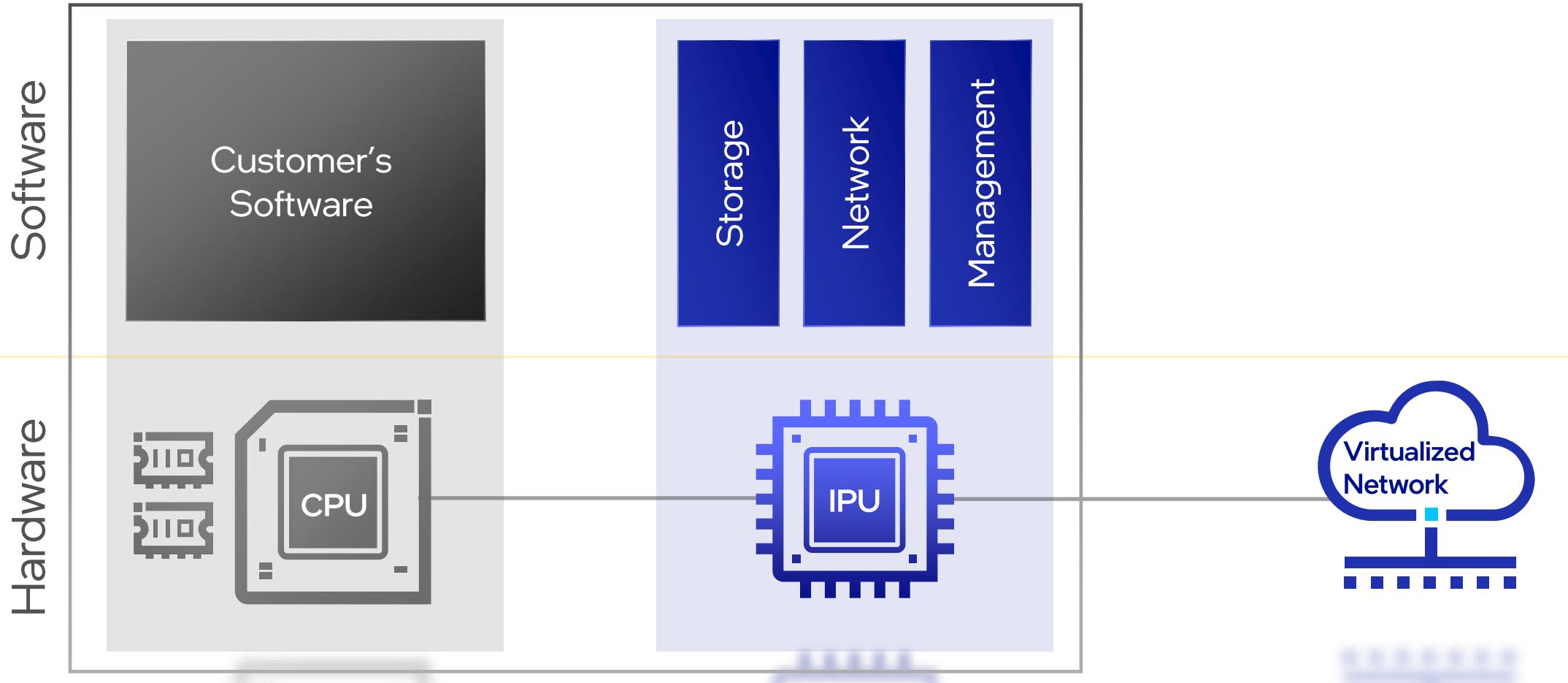
# Cloud Server Architecture





# Advantage 1 - Separation of Infrastructure and Tenant

Maximum Control and Isolation for the Tenant

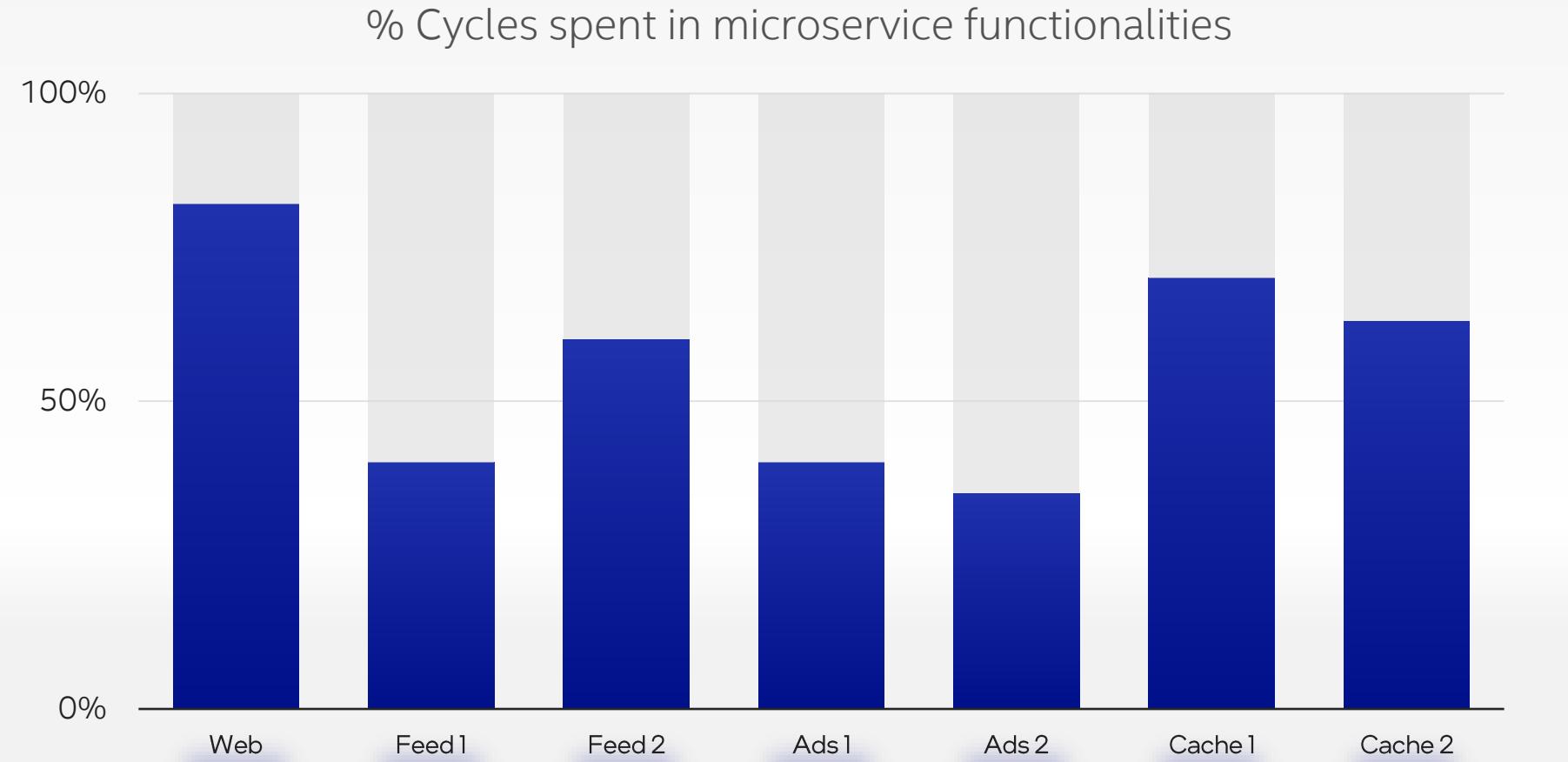


## Advantage 2 - Infrastructure Offload

In some cases, the majority of CPU cycles are spent on overhead

**31%  
to 83%**

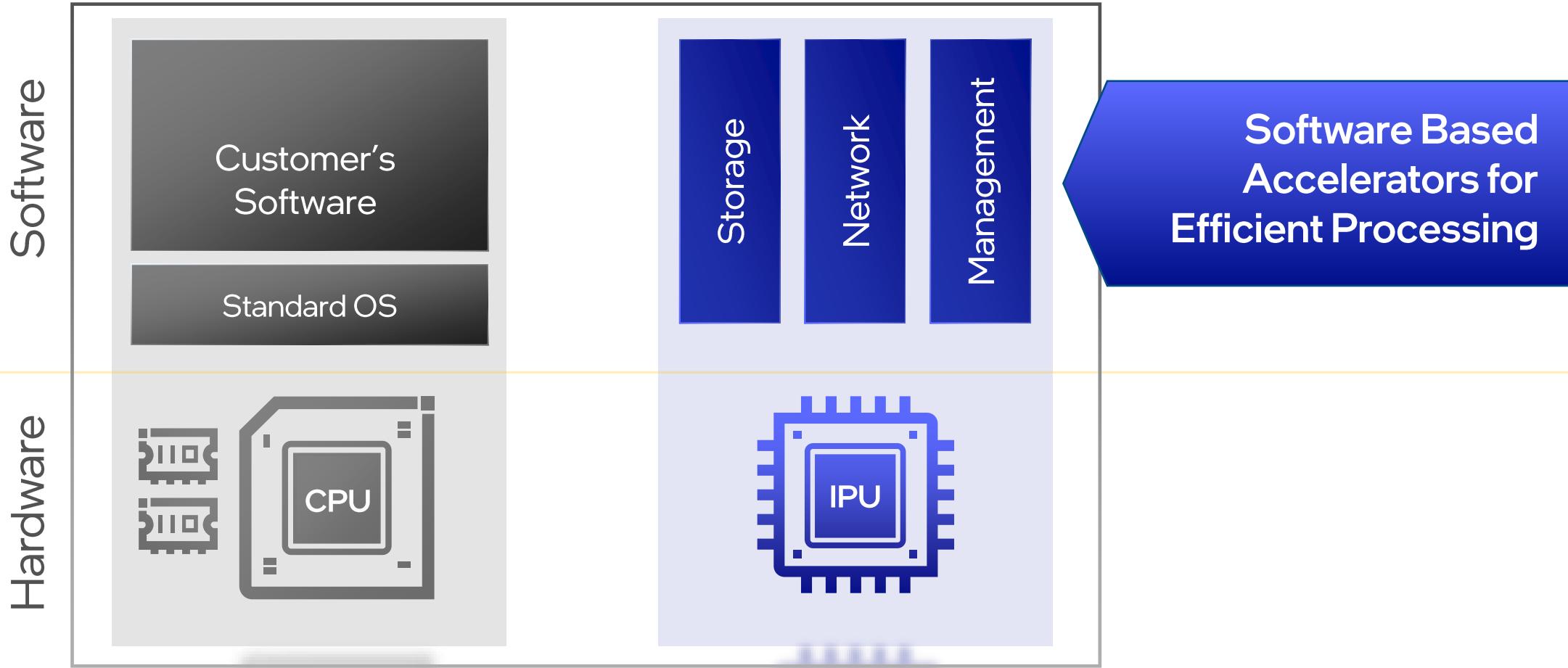
Microservice  
Overhead at  
Facebook



<https://research.fb.com/publications/accelerometer-understanding-acceleration-opportunities-for-data-center-overheads-at-hyperscale/>

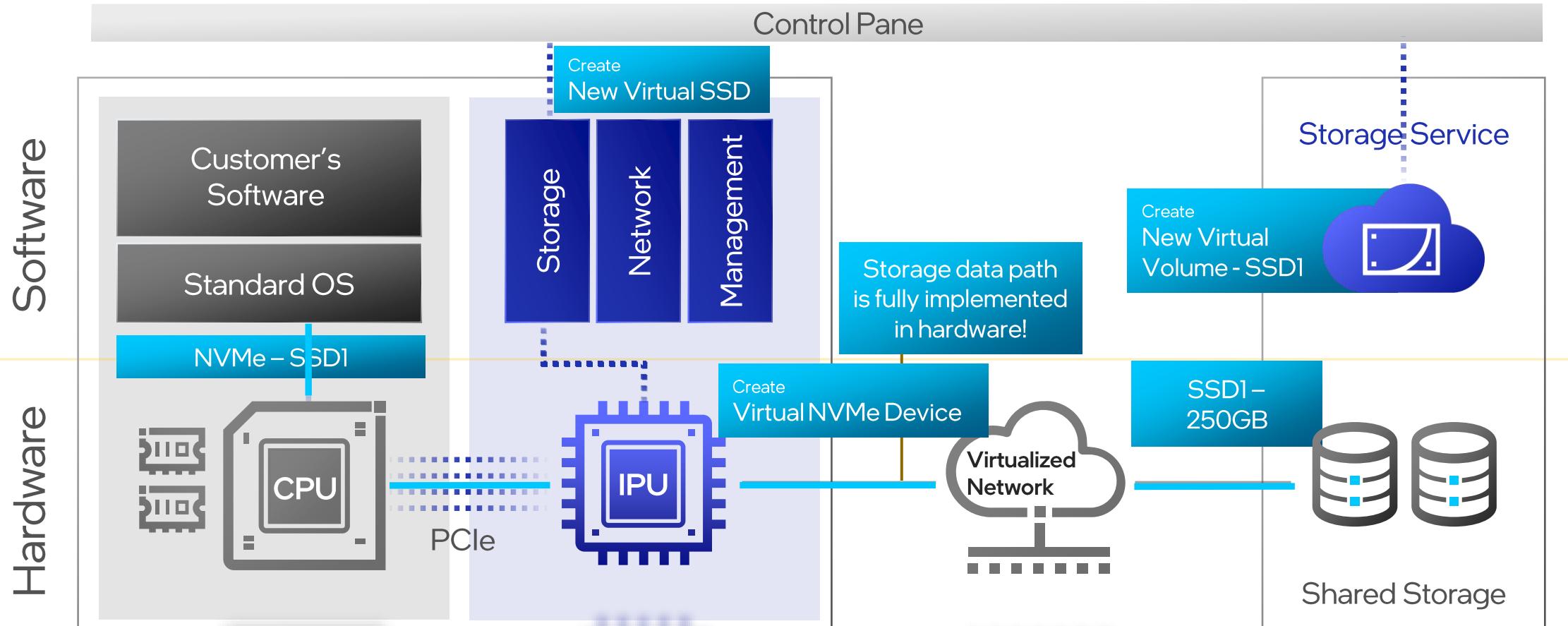
## Advantage 2 - Infrastructure Offload

Dedicated Accelerators Free up CPU Capacity



# Advantage 3 - Diskless Server Architecture

Scale with Virtual Storage via Network



# Broad Infrastructure Acceleration Portfolio

## Dedicated ASIC IPU

Performance and power optimized

Optimized secure networking and storage pipeline



## FPGA-based Acceleration

### IPU Platforms & Adapters

Faster time to market for evolving standards

Re-programmable Secure Datapath enables flexible/customizable workload offload (future proof)

Onboard Xeon processor



### SmartNICs

Programmable accelerated infrastructure workloads with customizable packet processing

Intel Ethernet NIC with DPDK support



# Partnering on the IPU



Introducing

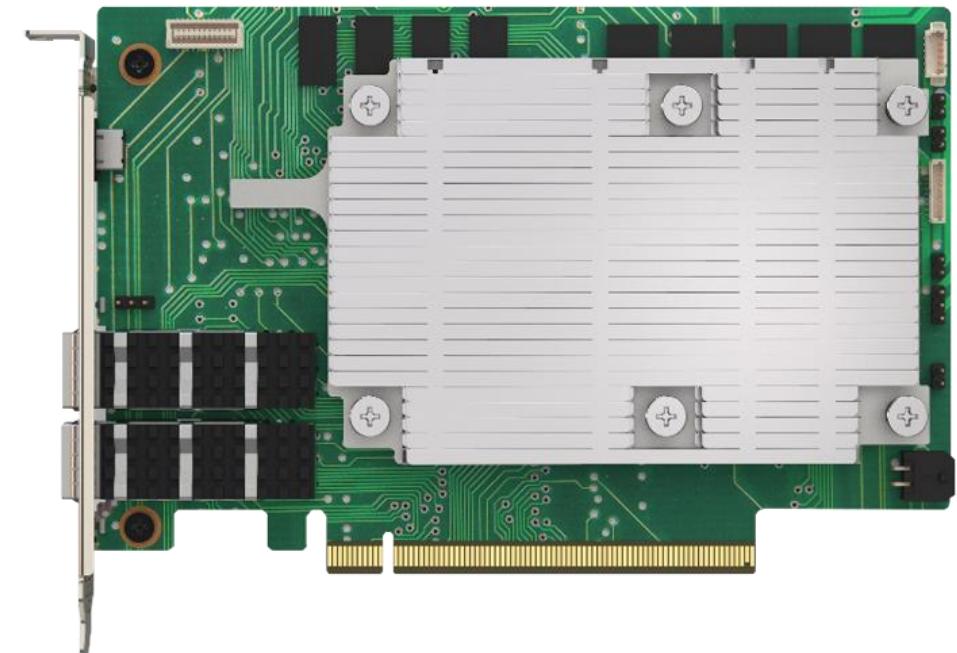
# Oak Springs Canyon

High perf networking and storage acceleration for  
Cloud Service Providers

OVS, NVMe over Fabric, and RoCE solutions

Programmable through Intel OFS, DPDK, and SPDK

Customizable solutions with FPGA



Intel OFS: Intel Open FPGA Stack

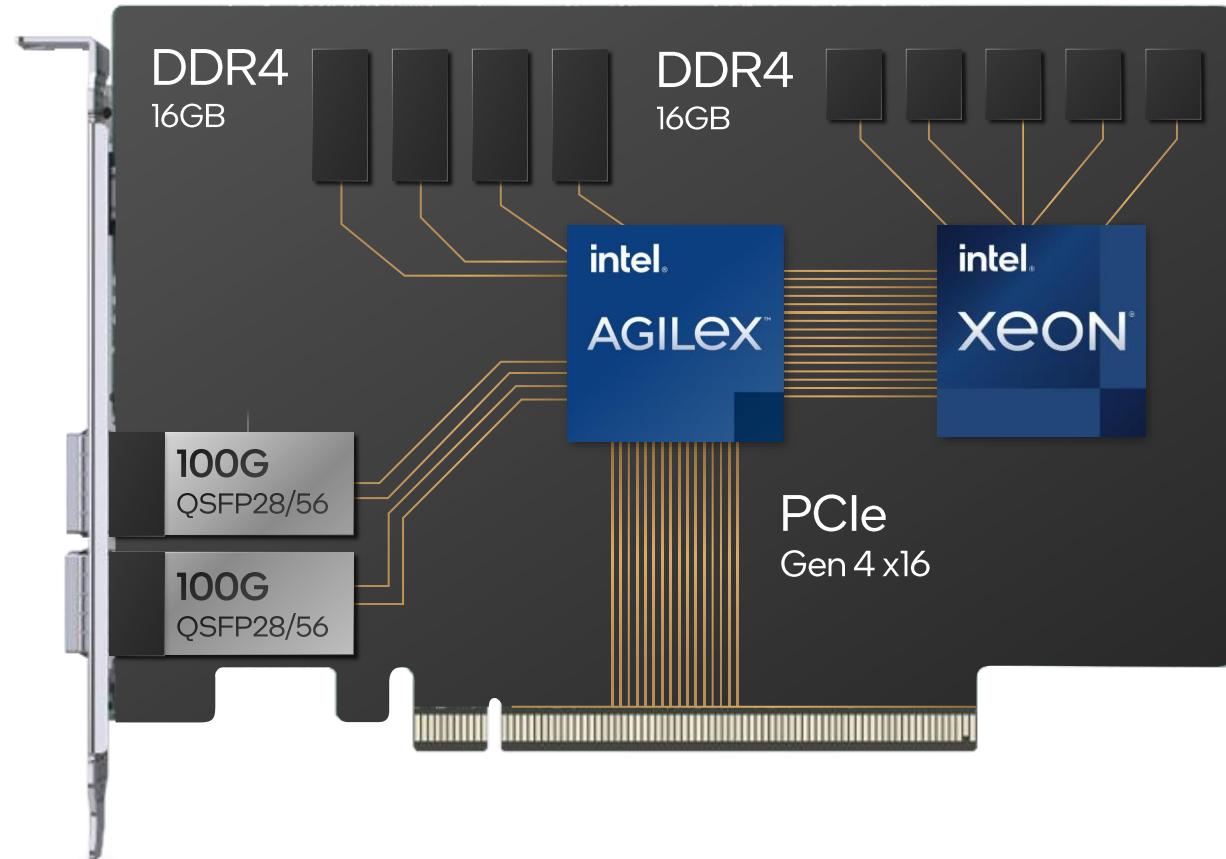
# Oak Springs Canyon

Built with Intel® Agilex™ FPGA and Intel® Xeon® D SoC

High speed Ethernet support - 2x100G

PCIe Gen 4 x16

Hardware crypto block enables security at line rate



Introducing

# Arrow Creek

Acceleration Development Platform (ADP) for  
High Performance 100G networking acceleration

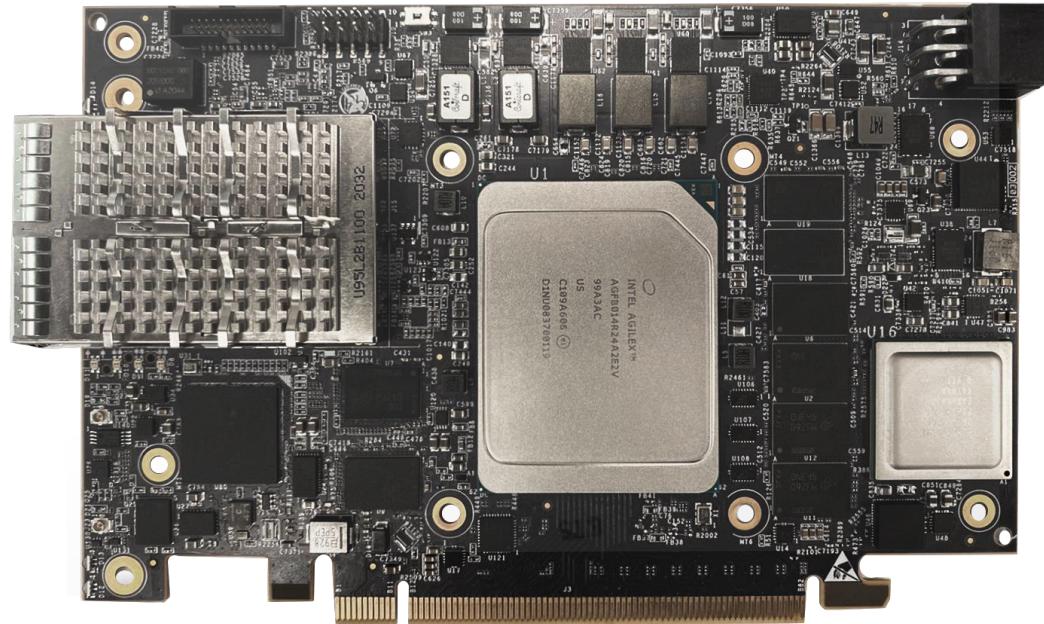
Customizable packet processing  
including bridging and networking services

Programmable through Intel OFS and DPDK

Accelerated infrastructure workloads  
Juniper Contrail, OVS, SRv6, vFW

Secure Remote Update  
of FPGA and Firmware over PCIe

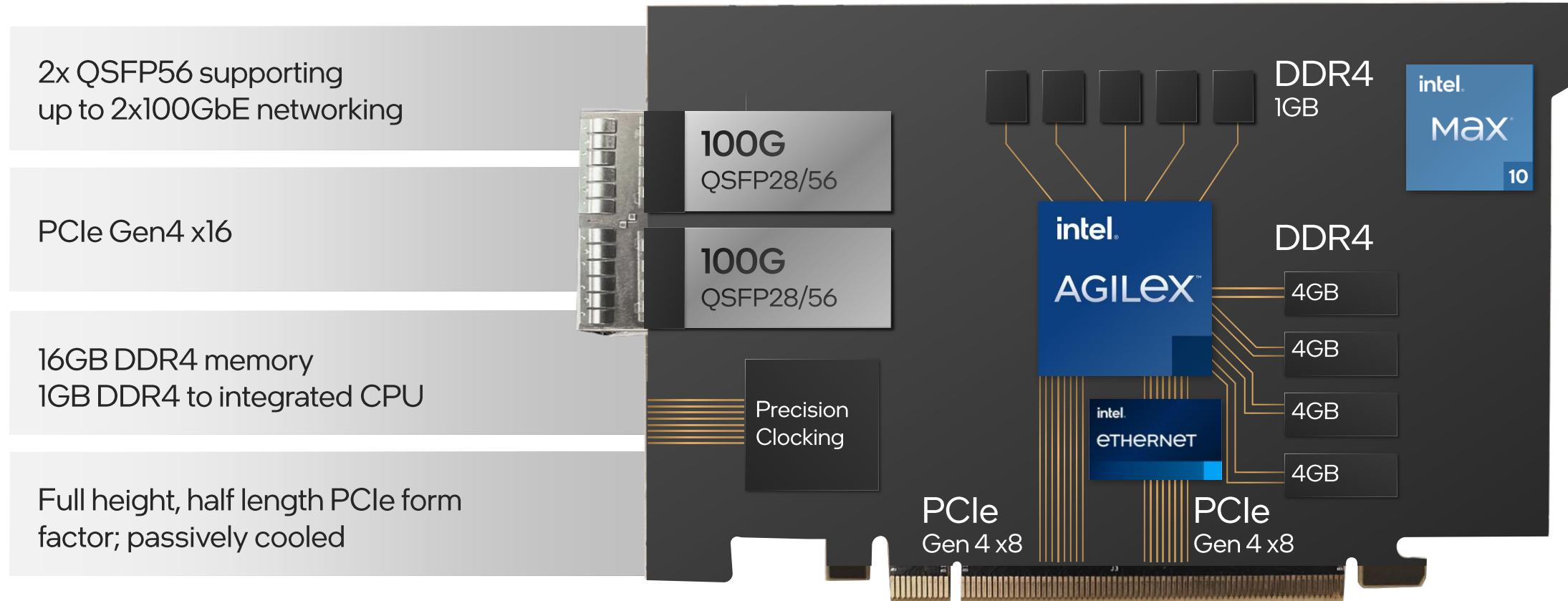
On-board root of trust



Intel OFS: Intel Open FPGA Stack

# Arrow Creek

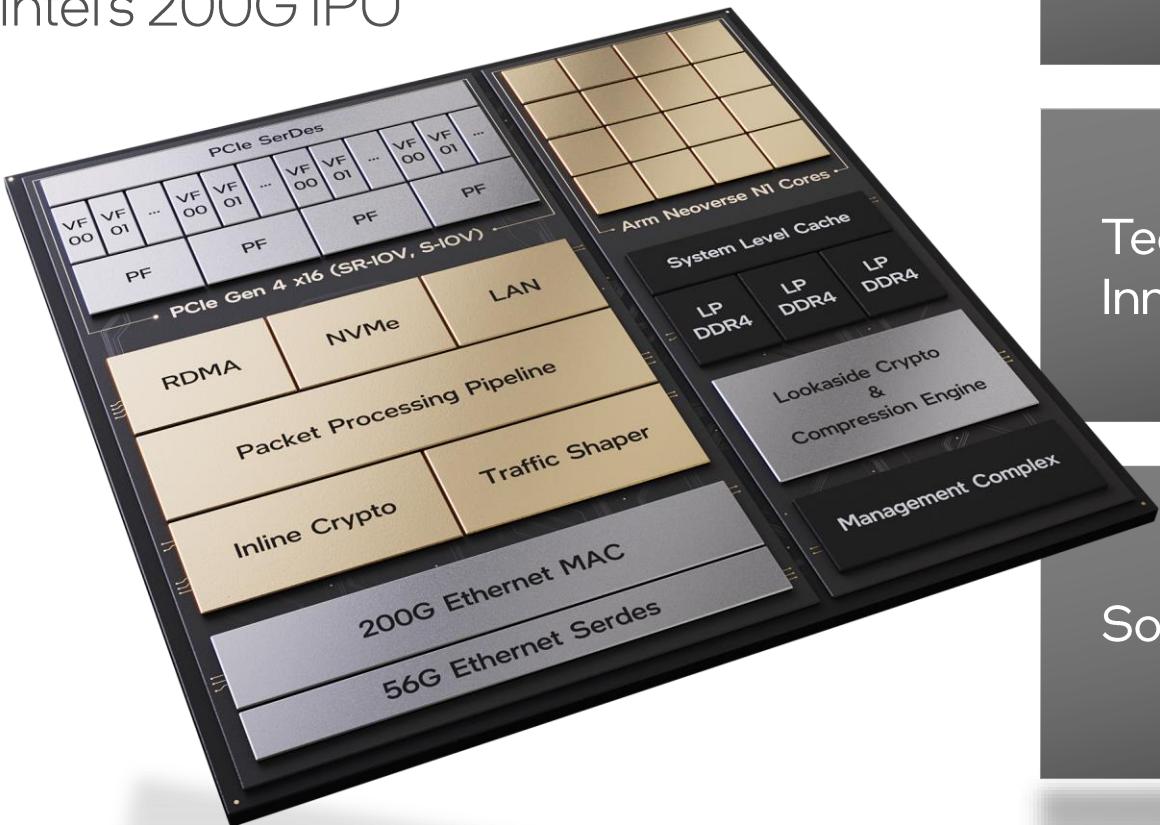
Built with Intel® Agilex™ FPGA and Intel® Ethernet E810 Controller



Introducing

# Mount Evans

Intel's 200G IPU



## Hyperscale Ready

Co-designed with a top cloud provider

Integrated learnings from multiple gen. of FPGA sNICs

High performance under real world load

Security and isolation from the ground up

## Technology Innovation

Best-in-Class Programmable Packet Processing Engine  
NVMe storage interface scaled up from Intel Optane Tech  
Next Generation Reliable Transport  
Advanced crypto and compression accel.

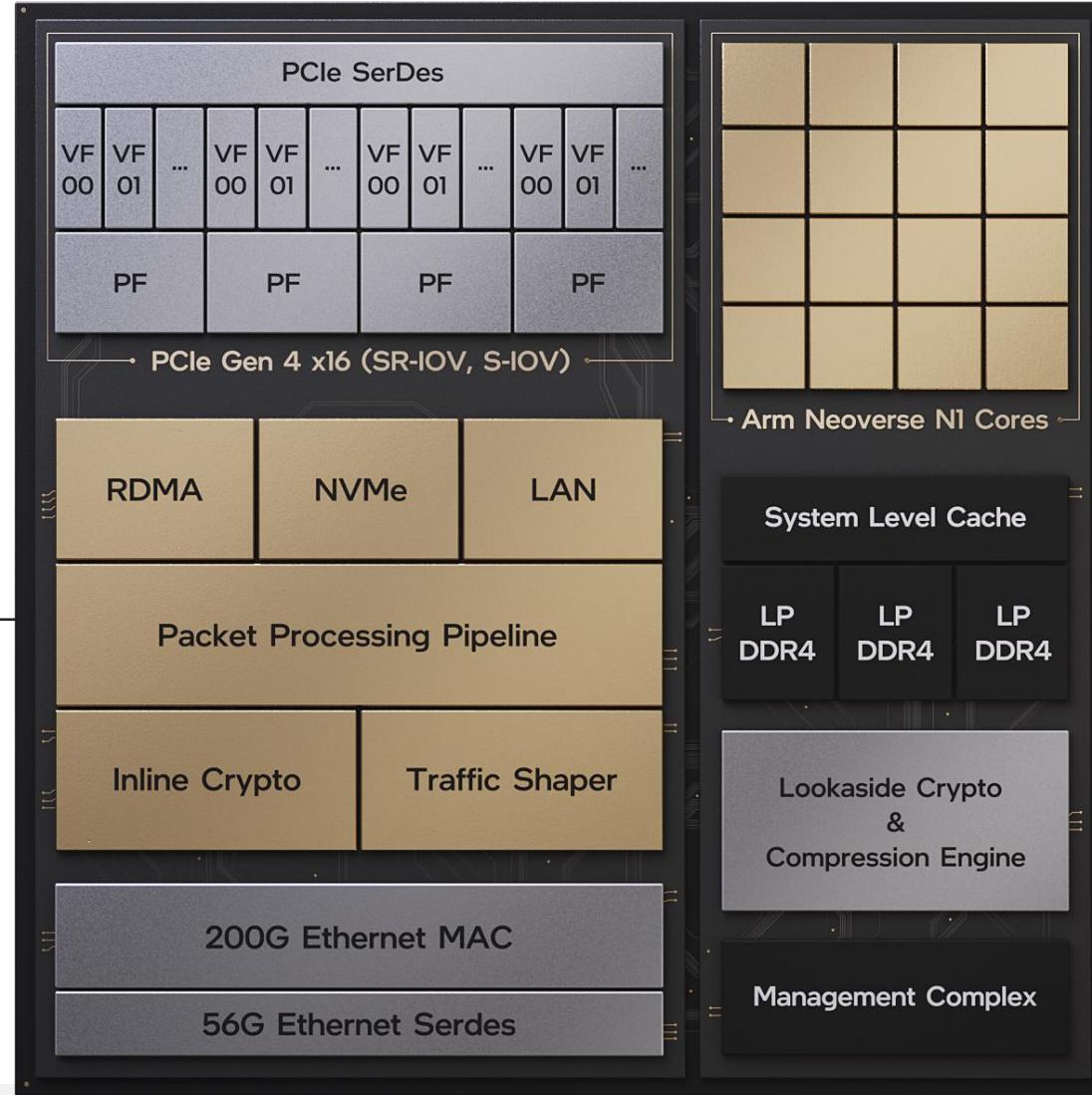
## Software

SW/HW/Accel co-design  
P4 Studio based on Barefoot  
Leverage and extend DPDK and SPDK

# Mount Evans

## Architectural Breakdown

Network  
Subsystem



# Mount Evans

## Architectural Breakdown

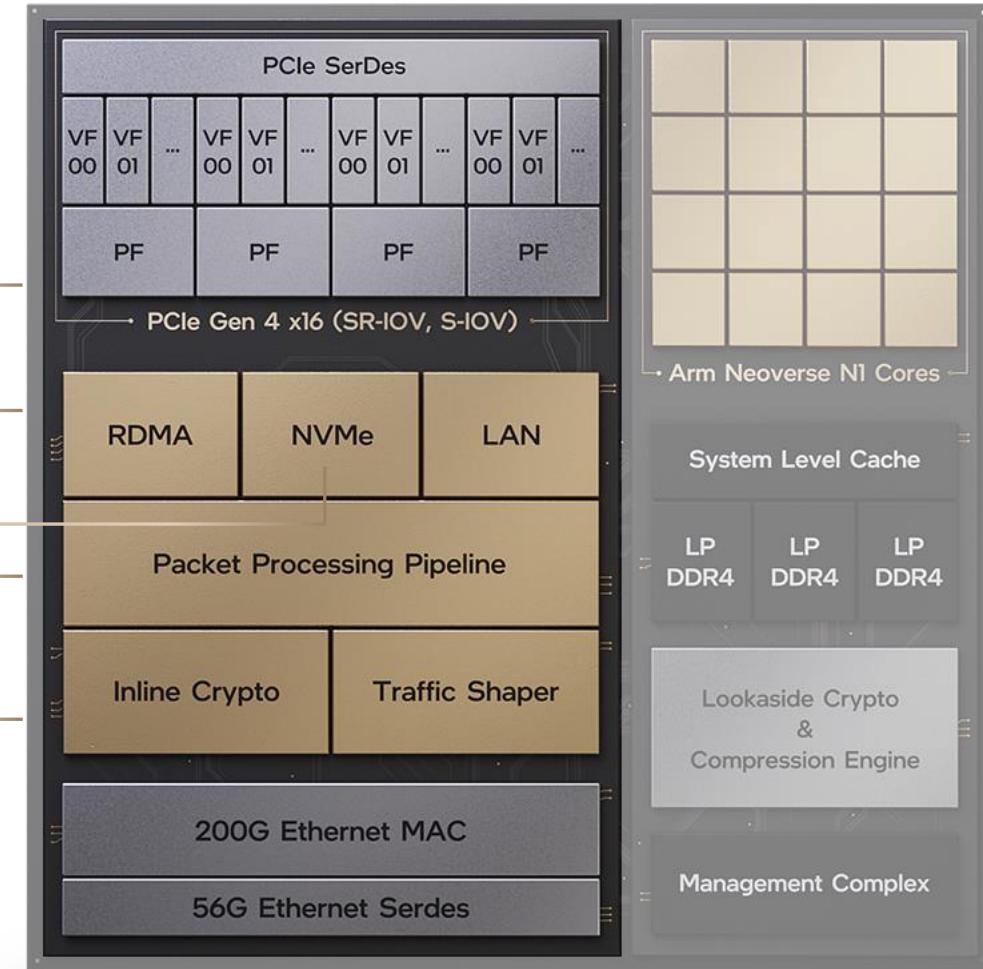
Support for up to 4 host Xeons with 200Gb/s full duplex

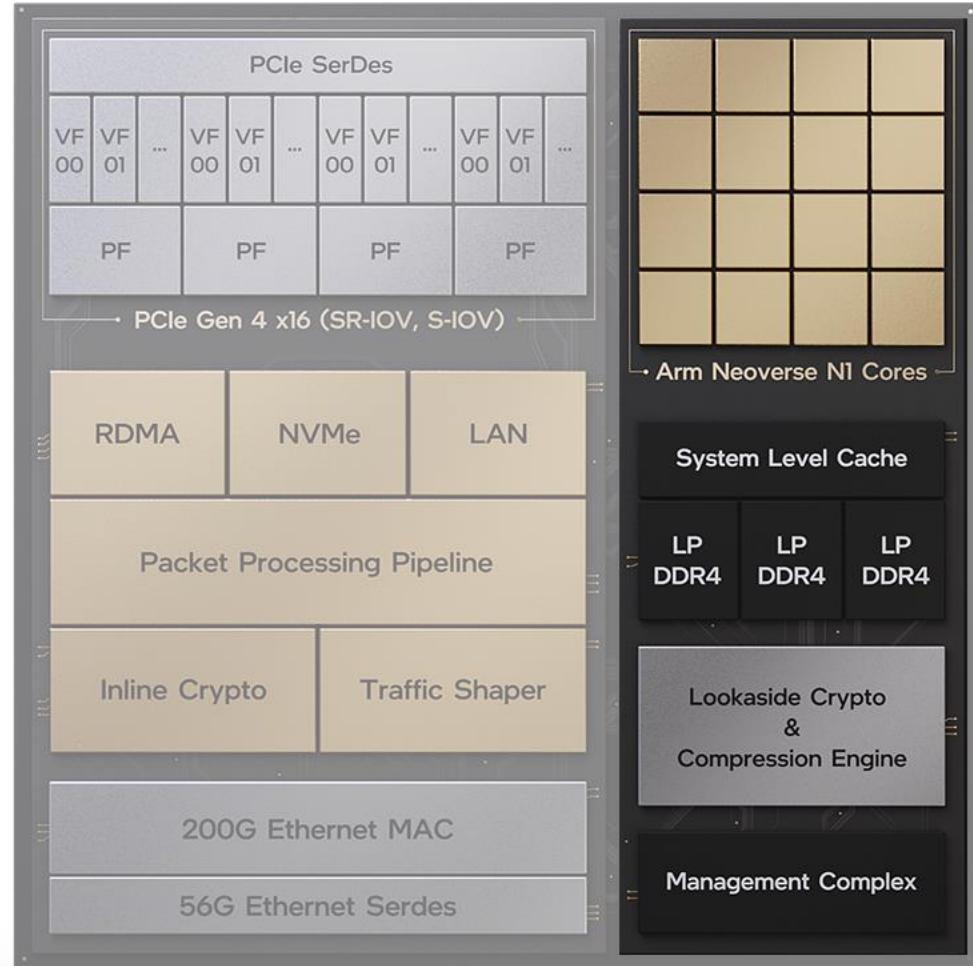
High-performance ROCEv2

NVMe offload engine

Programmable packet pipeline with QoS and telemetry capabilities

Inline IPSec





# Mount Evans

## Compute Complex

Up to 16 Arm Neoverse N1 Cores

Dedicated compute and cache with up to 3 memory channels

Lookaside crypto and compression

Dedicated management processor

# Summary

- Cloud service providers maximize data center revenue by offloading infrastructure tasks including storage, networking and management functions from CPUs to IPUs
- Intel is the volume leader in IPU deployments at major CSP's
- SmartNICs and IPU platforms for cloud and comms service providers are available today

[Intel.com/IPU](https://Intel.com/IPU)

# Questions?

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**Sabrina Gomez, Director Programmable Solutions Group Marketing**

[Sabrina.Gomez@intel.com](mailto:Sabrina.Gomez@intel.com)

The Intel logo is displayed in white on a solid blue background. The word "intel" is written in a lowercase, sans-serif font. A small, solid blue square is positioned above the letter "i". The letter "i" has a vertical stroke on its left side. The letter "t" has a vertical stroke on its right side. The letter "e" has a vertical stroke on its left side. The letter "l" has a vertical stroke on its right side. A registered trademark symbol (®) is located at the bottom right of the "l".