Silicom Ltd.

Connectivity Solutions

Tailor Made Solutions | Off-the-shelf Products | Innovative Solutions

Optimizing vRAN with Intel® FPGA Platform

Silicom Product Line

- Silicom overview
- Silicom Open RAN offerings
- N6010/N6011 Introduction
- Silicom Time Synchronization

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Founded in 1987

A public company
NASDAQ(SILC)

O-RAN ALLIANCE

HQ, R&D and manufacturing facilities are in Israel, with offices in the US, Denmark and China

33 years of experience in networking and connectivity

TELECOM INFRA PROJECT

>300 employees

Collaboration with Strategic partners

OPEN Compute Project

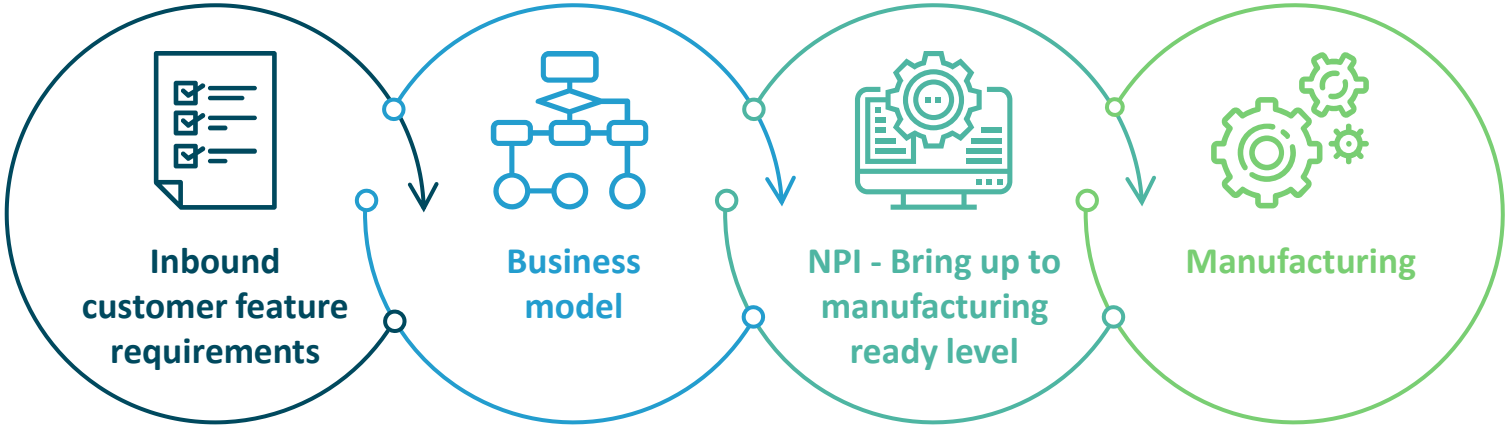
Over 300 clients worldwide

Intel SOC and FPGA Design House

FPGA design experts both HW and IP cores

TIP, ORAN, OCP

Rapid Innovation (Process)



Inbound customer feature requirements	Business model	NPI - Bring up to manufacturing ready level	Manufacturing
Active collaboration	Assessment of potential	Big engineering team	Flexible Locations:
HW and SW R&D evolvement	Flexible	Define Manufacturing procedure	Israel
Production evolvement	No NRE, only PO	Define Testing procedure	China
Partner up if necessary	Time table	Define QA	Philippines
33 yr. experience in networking solution designs	Quotation	Certifications	US
			India

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Silicom Products Overview for Mobile Infrastructure

4G/5G Edge (UE) for FWA market

4G/5G DU and CU platforms

4G/5G Add-in cards for DU and CU

- Silicom Madrid and Cordoba – ATOM platform with LTE and 5G uplink for Fixed Wireless Access
- Silicom Barcelona – 1U Xeon platform including Time Sync and FEC acceleration
- Silicom Vigo – 2U Xeon platform including Ethernet Switch
- Silicom Palma - 2U Xeon platform including Time Sync and FEC acceleration
- Silicom STS - Ethernet NIC with Time Sync technology
- Silicom N6010 - SmartNIC (FPGA) with Silicom Time Sync technology
- Silicom Lisbon – 4G/5G FEC acceleration
- Silicom N5014 – 5G Core UPF acceleration based on FPGA technology

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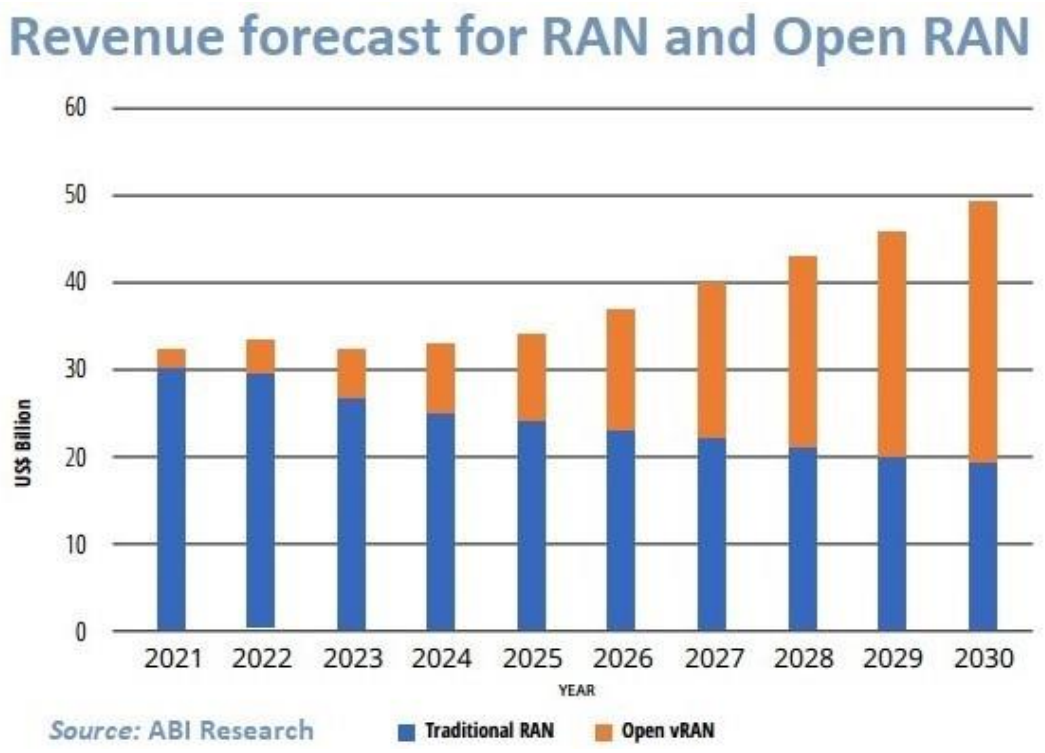
Open RAN Market Today



2022: We are here

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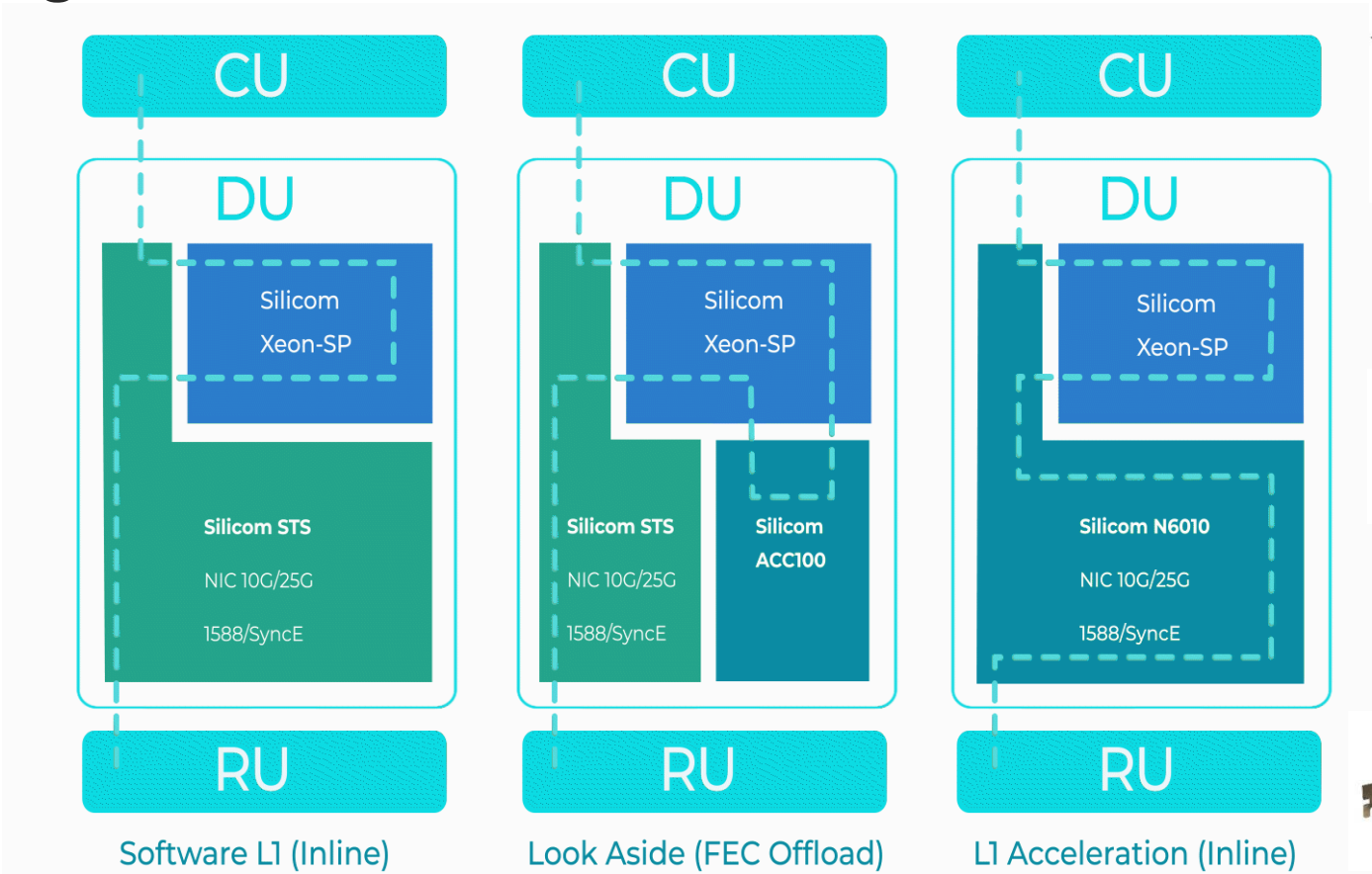
Scaling – Software vs Hardware acceleration



ACC100

Time Sync NIC

N6010/N6011

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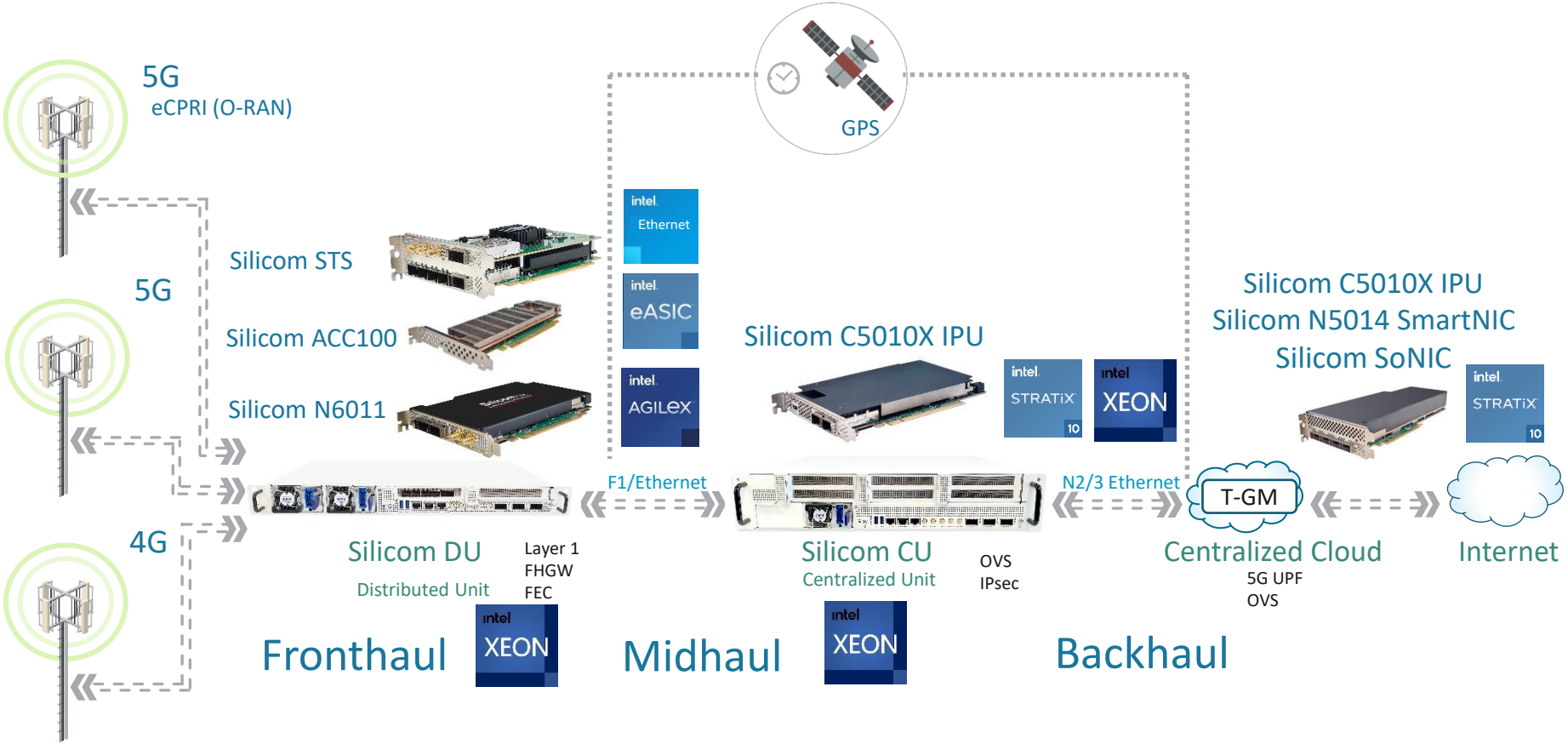
Silicom Disaggregated 4G/5G Solutions – from Edge to Cloud



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Silicom FPGA SmartNIC N6010/N6011

SmartNIC For NFVi, VNF, vRAN, OpenRAN

High performance networking acceleration card Programmable through Intel® DPDK and OPAE Accelerated Workloads

- Intel Open FPGA Stack (OFS)
- Support for vRouter, OVS, SRv6, UPF, vFW acceleration
- 4G and 5G vRAN enablement package, DPDK/BBDev and FlexRAN

Built with Intel® AgileX AGF014 FPGA

- High speed Ethernet support : 100G, 25G, and 10G
- Supports SyncE, CPRI, eCPRI
- PCIe Gen 4 x16(N6010) 2 x8(N6011)
- 16GB DDR4 memory, 1GB DDR4 to HPS
- BMC for monitoring and control (PLDM)
- Front panel SMAs for IEEE1588 1pps and master clocking
- O-RAN LLS-C1, -C2, -C3 support
- Full Height, ½ Length, PCIe card
- Optimized for 75W-100W TDP

Supports Intel® Ethernet Controller E810

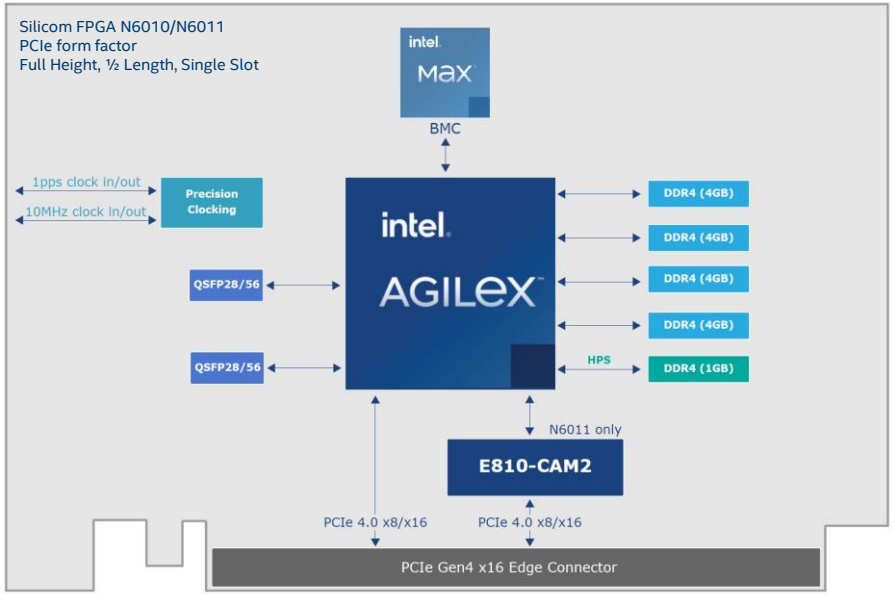
- Extensive OS support and easier system integration
- Dual 100Gbps pipeline

Arrow Creek SKU

- Silicom FPGA SmartNIC N6010 (base)
- Silicom FPGA SmartNIC N6011 (base + Intel NIC)

Base

Hard NIC



The FPGA for the Data-Centric World

intel AGILEX

PROCESS DATA	~2X Increased Fabric Performance per Watt[1,4]	Average **45%** Higher Performance[2,4]	Up to **40%** Lower Power[2,4]	Up to **40 TFLOPS** DSP Performance[3,4]
STORE DATA	DDR5 & High Bandwidth Memory (HBM)	INTEL® OPTANE™ Persistent Memory Support		
MOVE DATA	Hard IP : 400G Ethernet, Compute Express Link (CXL)[5] and PCIe Gen4/5 x16	32/56/116G Transceiver Data Rates		

Compared to competing 7 nm FPGA
[2] Compared to Intel® Stratix® 10 FPGAs
[3] With FP16 configuration
[4] Based on current estimates
[5] Consult rollout schedule
See FPGA - Performance Index for workloads and configurations. Results may vary.

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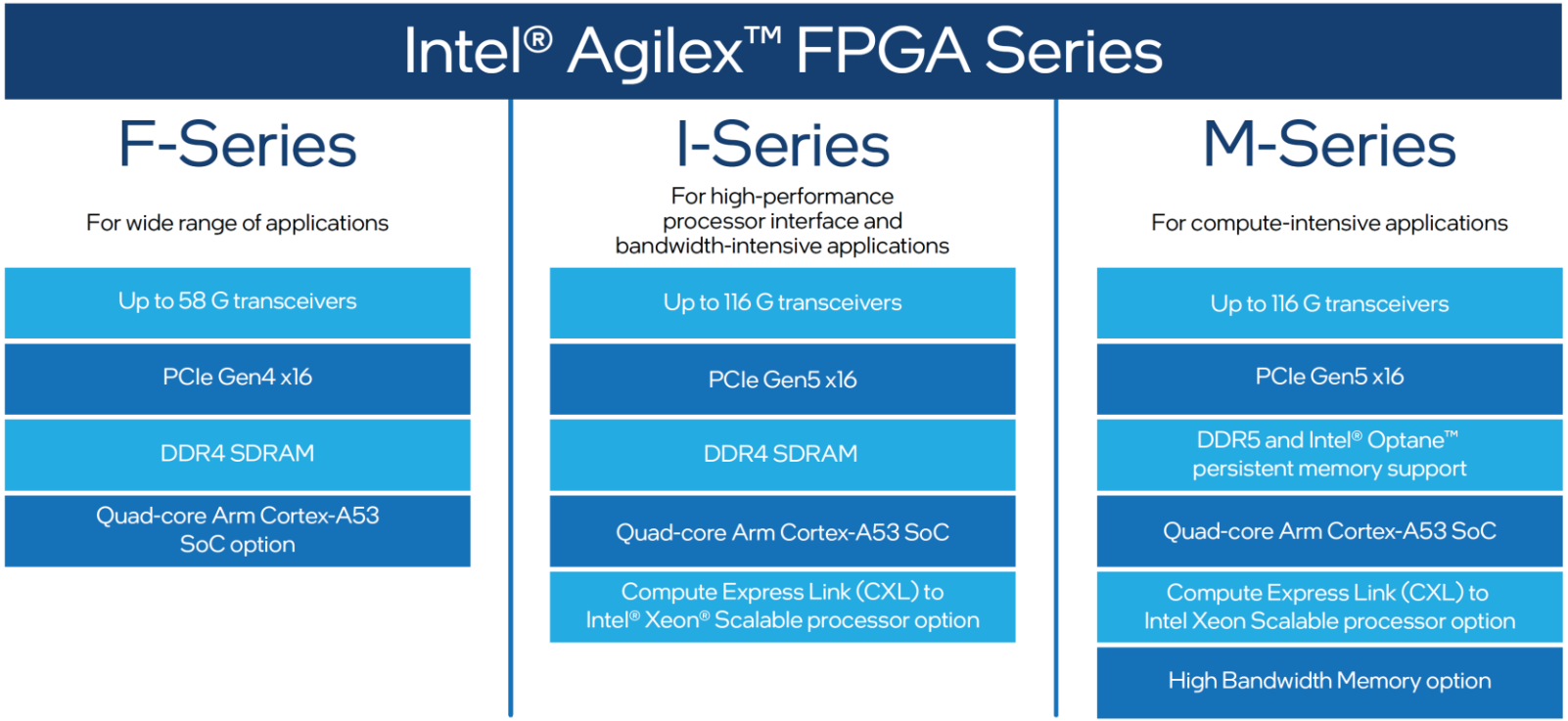
Intel Agilex Architecture



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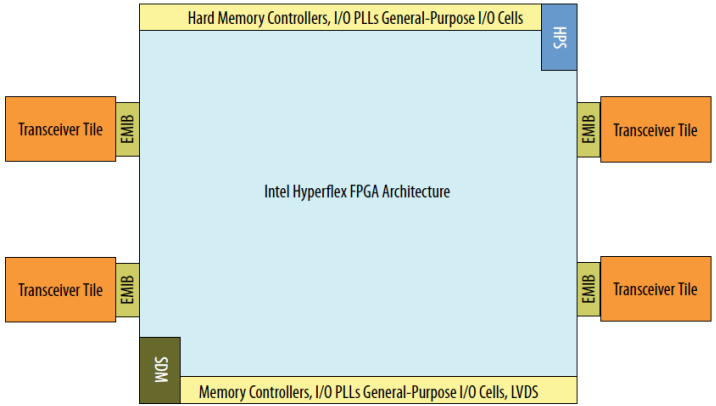
Intel Agilex F014 Specification

Table 3. Intel Agilex F-Series FPGAs and SoCs Family Plan Part-1

Intel Agilex F-Series Device Names	Logic Elements (LE)	eSRAM Blocks	eSRAM Mbits	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	Variable Precision DSP Blocks	18x19 Multipliers
AGF 006	573,480	0	0	2,844	56	9,720	6	1,640	3280
AGF 008	764,640	0	0	3,792	74	12,960	8	2,296	4592
AGF 012	1,178,525	2	36	5,900	115	19,975	12	3,743	7486
AGF 014	1,437,240	2	36	7,110	139	24,360	15	4,510	9020
AGF 022	2,208,075	0	0	10,900	212	37,425	23	6,250	12500
AGF 027	2,692,760	0	0	13,272	259	45,640	28	8,528	17056

Intel Agilex FPGA Block Diagram



Intel® Ethernet Controller E810

Performance for Cloud Applications

Delivers the bandwidth and increased application throughput required for demanding cloud workloads including edge services, web servers, database applications, caching servers, and storage targets.

Optimizations for Communications Workloads

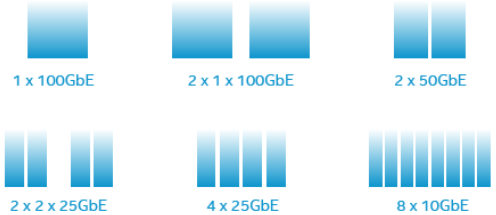
Provides packet classification and sorting optimizations for high-bandwidth network and communications workloads, including mobile core, 5G RAN, and network appliances.

Supports Hyperconverged Solutions

The 800 Series broad portfolio of adapters, with different port counts and form factors, delivers performance with efficient use of server processors.

Flexible port and speed combinations

EPCT, available on 100GbE 800 Series Network Adapters[1], offers a versatile solution for high-density, port-constrained network environments. One port becomes eight 10GbE ports, four 25GbE ports, and more–up to six configurations to choose from.



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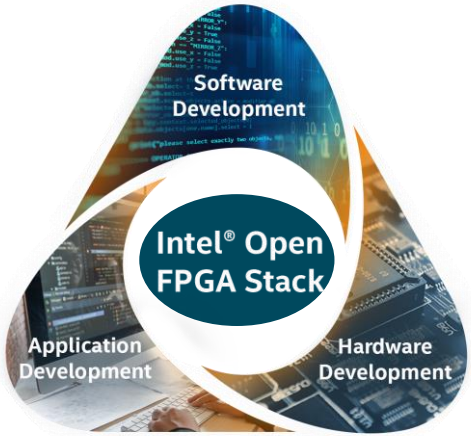
OFS – Open FPGA Stack

Intel® OFS for Custom Platform Development

2nd Generation of Intel® FPGA Platform Software



- **Ecosystem** of Intel® Open FPGA Stack-based boards, workloads, and OS distributions
- **Scalable**, source-accessible hardware and software **infrastructure**
- **Customization** of FPGA design with modular and composable source code
- **Adoption** of upstreamed kernel software by leading OS and orchestration vendors

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Silicom OFS Offerings

A scalable hardware and software infrastructure that includes:

Hardware

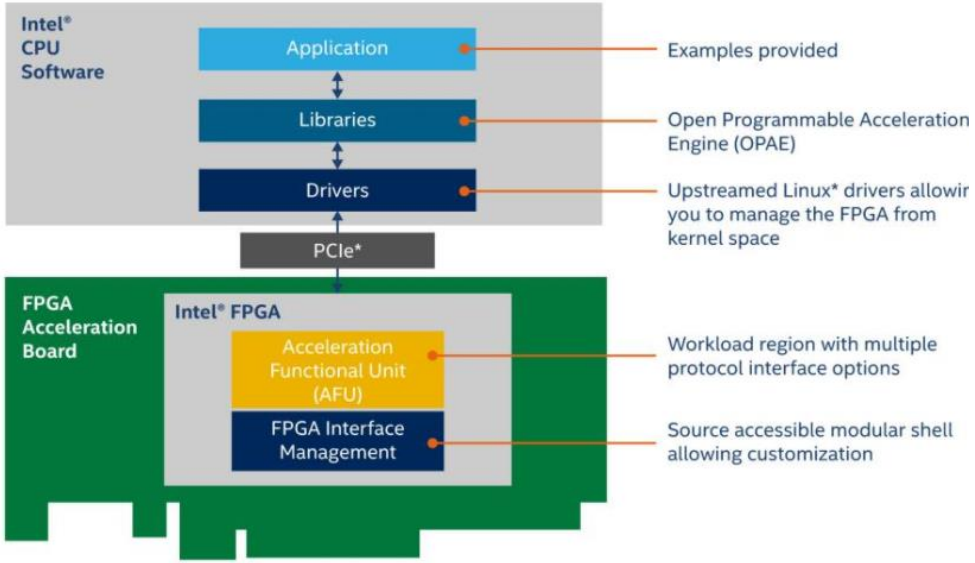
- Acceleration Functional Unit (AFU) Region for Workload Development with Sample AFUs
- FPGA Interface Manager (FIM)
- Board Management Controller (BMC)
- HLD enablement

Software

- Upstreamed, open-source kernel drivers
- OPAE libraries, tools and APIs
- Example Applications

UVM Test Environment

- Verification environment provided through Git repositories



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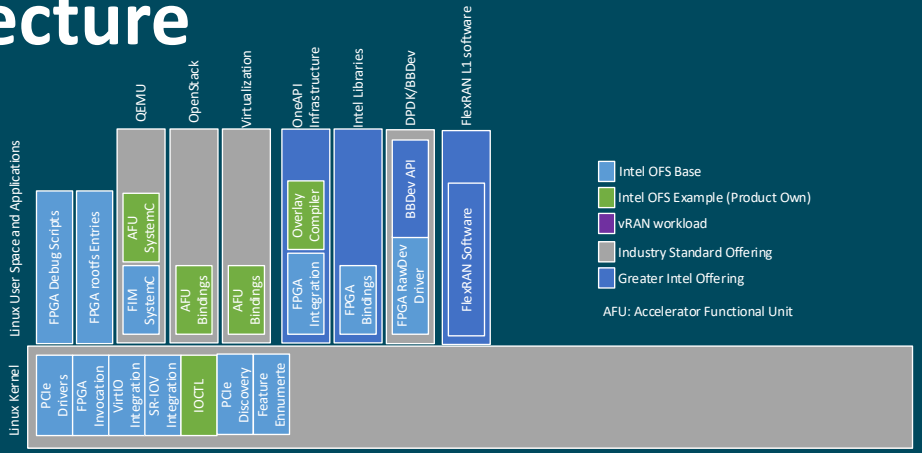
Intel® OFS System Architecture

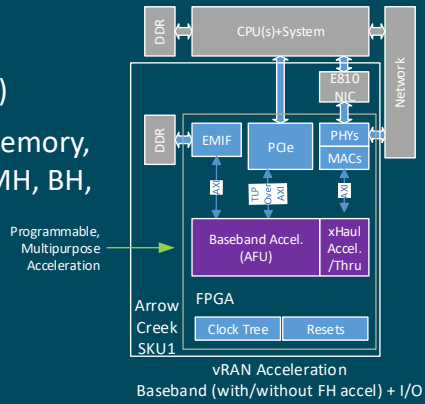
Software

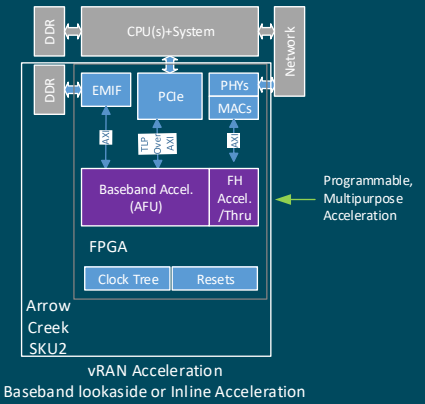
- Upstreamed OS kernel support
- Runtime & drivers
- Libraries & application software
- Virtualization
- Simulation



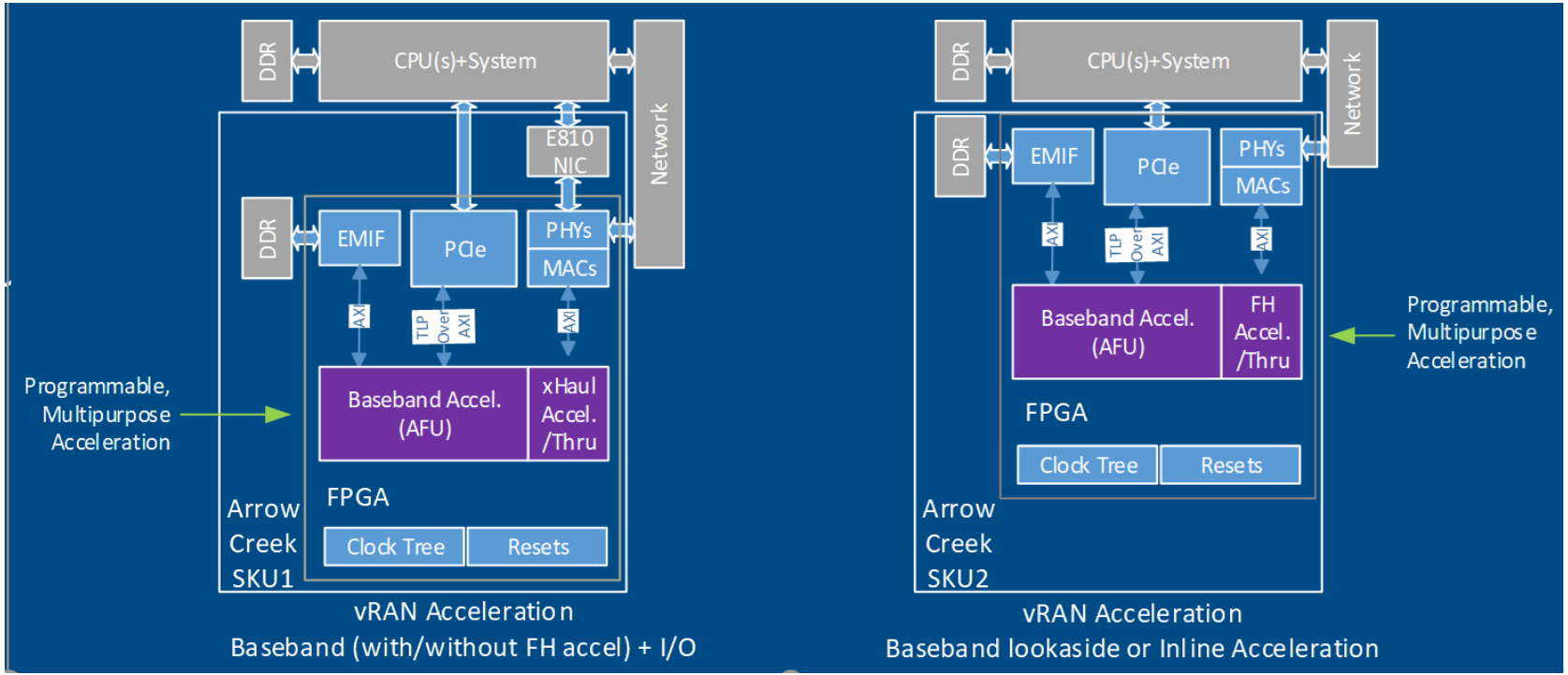
Hardware

- Modular, composable FPGA Interface Managers (FIMs)
- Provides interfaces between board resources (PCIe, memory, networking, etc.) and acceleration function unit (FH, MH, BH, FEC, etc.)
- Supports partial reconfiguration





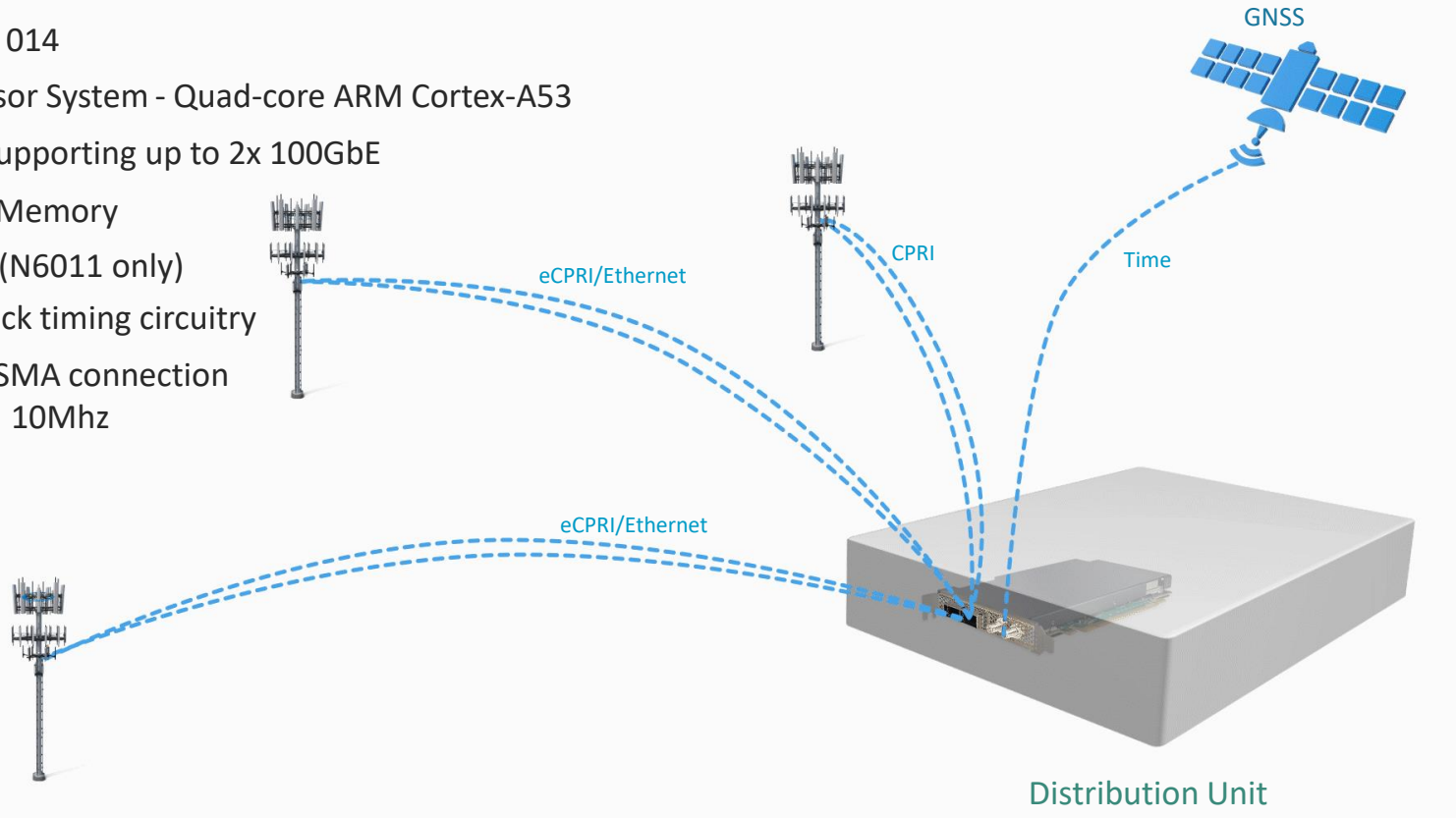
Block Diagram



vRAN Acceleration

How N6010/N6011 improves TCO, CAPEX and OPEX

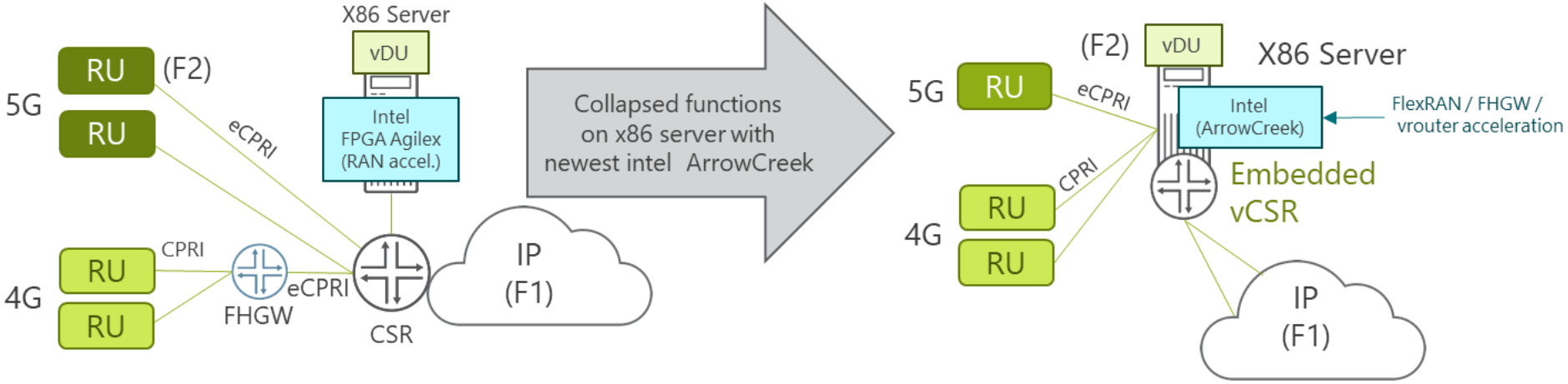
- ✓ Agilex™ AGF 014
- ✓ Hard Processor System - Quad-core ARM Cortex-A53
- ✓ 2x QSFP28 supporting up to 2x 100GbE
- ✓ 16GB DDR4 Memory
- ✓ E810-CAM2 (N6011 only)
- ✓ Precision clock timing circuitry
- ✓ Front panel SMA connection for 1PPS and 10Mhz



vCSR

Optimised Edge site integration in non standalone 5G deployments.

- Legacy 4G requires cPRI to eCPRI conversion (FHGW)
- FHGW + CSR for routing integration and F2 aggregation toward vDU



Use Case: 5G vRAN

Silicom FPGA SmartNIC N6010/1 Platform with 5G vRAN workload (FEC + xHaul); single PCIe Gen4 x16 slot:

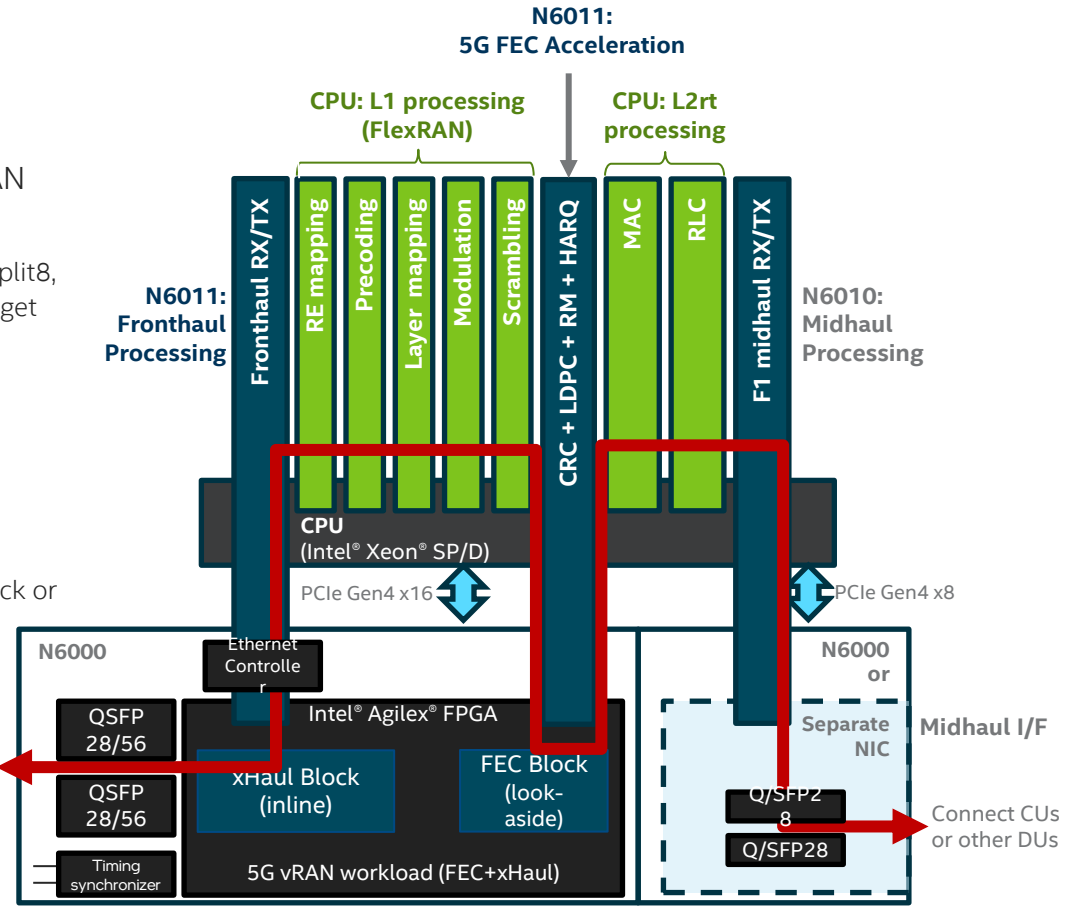
1. Fronthaul I/F: 8x10GE, 2x2x25GEs, 2x100GEs, Split 7-2x or Split8, O-RAN C3, C2 and C1 Timing Configuration (1588 GM/BC, target <10ns accuracy), CPRI support, SyncE
2. FEC processing: LDPC Gen 3.0 (URLLC support) encoder and decoder, Rate Match, De-Rate Match, HARQ, CRC, TB-CB conversion

3rd Gen Intel® Xeon® Scalable Processor

- L1 and L2rt functions in software (Intel FlexRAN reference stack or customer's own)

vRAN use case example*:

- 24-36 cells 4T4R 20MHz, FDD, Narrow Band
- 3-6 cells 64T64R 100MHz, TDD, MidBand, mMIMO
- DRAN, CRAN, Private RAN



5G vDU use case (L1 + L2rt) high level abstraction
Not all functions listed, different L1 splits may apply

** Performance varies depending on traffic model definition. See Performance Estimates slide in Appendix*

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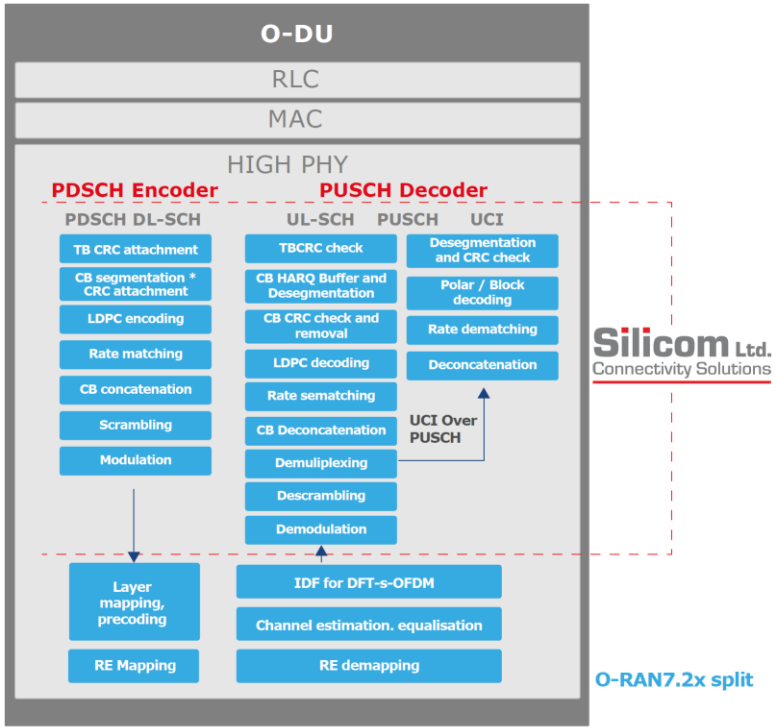
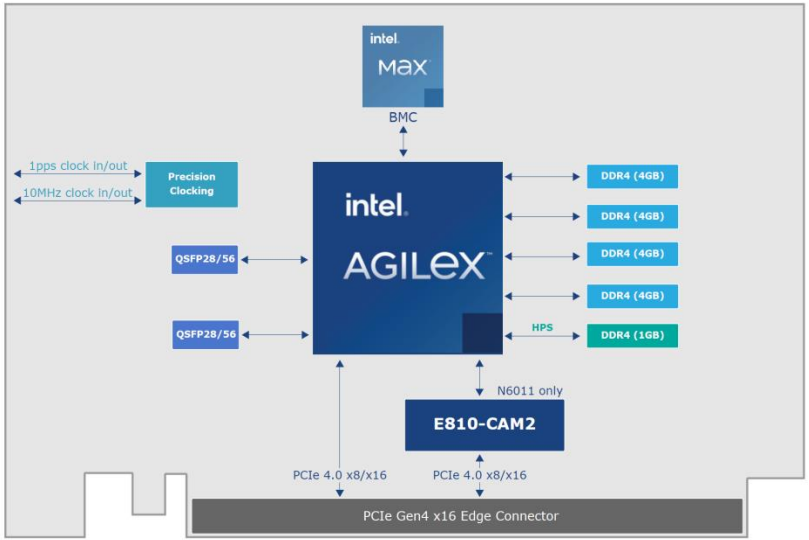
Layer 1 High Phy Offload IP





O-RAN 7.2x Split Description between O-DU and O-RU

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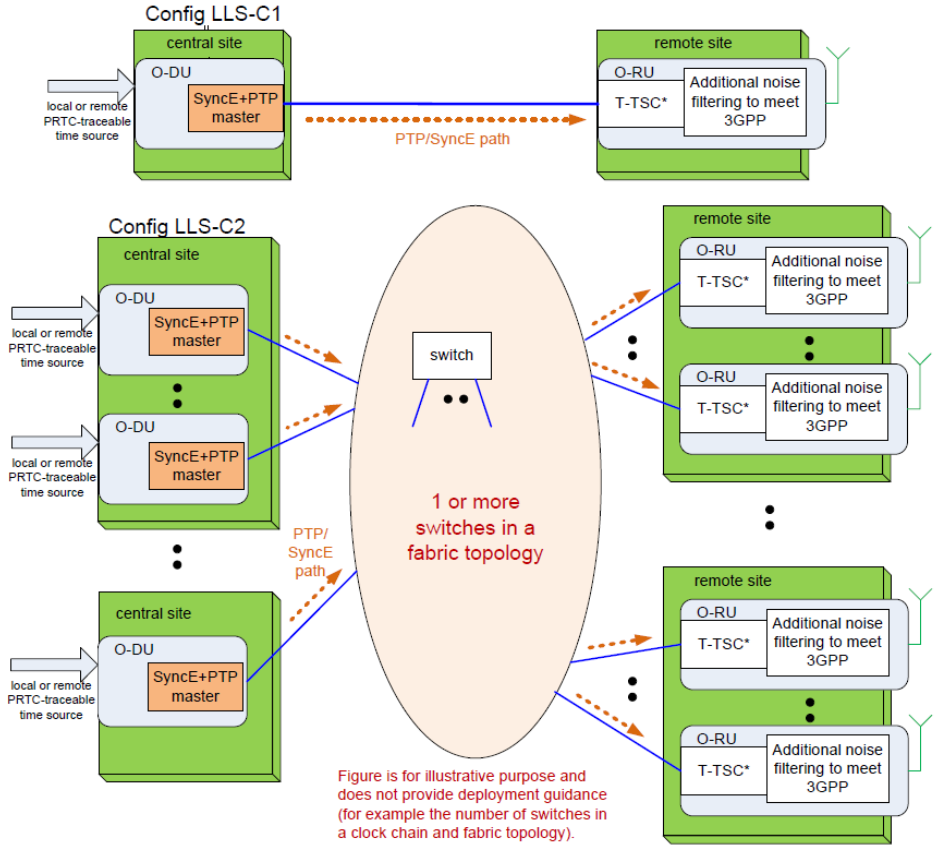
STS – Silicom Time Synchronization IP

STS
Silicom Time Sync
Technology

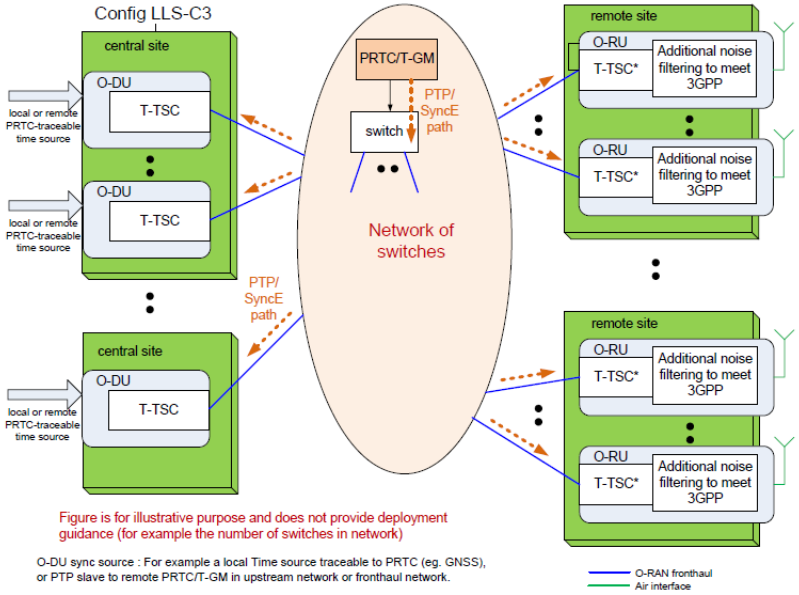
What problem we come to solve?

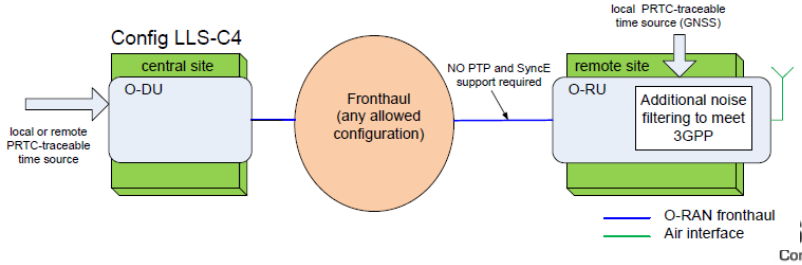
- O-RAN Low Level Split C1 and C2 requires DU to support PTP and SyncE.
- DU need to support PTP/1588 and SyncE
- In some config DU needs to be GM
- Target ORAN LLS-C1 and C2



What problem we come to solve?

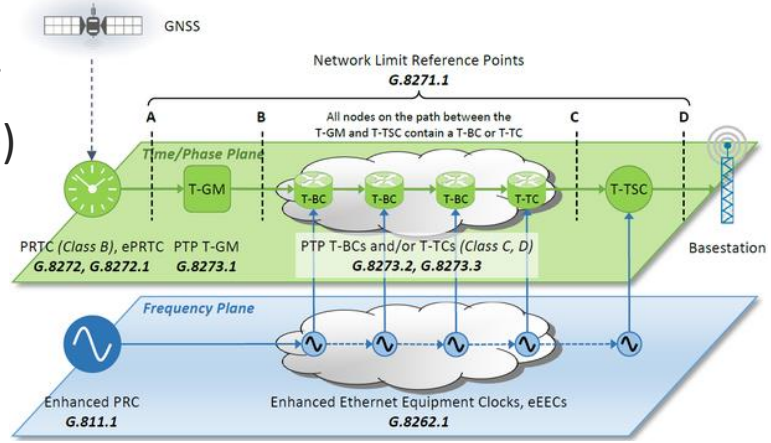
- LLS-C3 - using a switch with PRTC/GM and SyncE
  - Problem: high-cost switch that effect both CAPEX and OPEX.
- LLS-C4 – no PTP/SyncE support
  - Problem: cannot meet the requirements needed to support URLL and mMIMO.





Time Synchronization Standards of STS

- 1588/PTP over IPv4 / IPV6, IEEE1588v2
- SyncE /ITU-T G.8262
- T-BC/T-TSC Boundary Clock and TSC Slave Clock /G.8273.2
- T-GM Grand Master /G.8273.1 per G.8275.1 PTP Profile
- PRTC Primary Reference Time Clock Class B/G.8272
- OC Own Clock(Master / Slave) – Class C(Stratum 3e)
- BMCA - Best Master Clock Algorithm
- 1.5usec TIE at <4 Hours Hold Over
- Software 1588 Stack and Servo SW in x86/ARM



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THANK YOU

www.silicom-usa.com

Nadav Yafe, VP Product
nadavy@silicom.co.il

Oren Benisty, VP Sales
orenb@silicom.co.il