

# Intel® Network Builders Insights Series

## The Full vRAN Experience

Daniel Lynch, FlexRAN Senior Marketing Director, Intel



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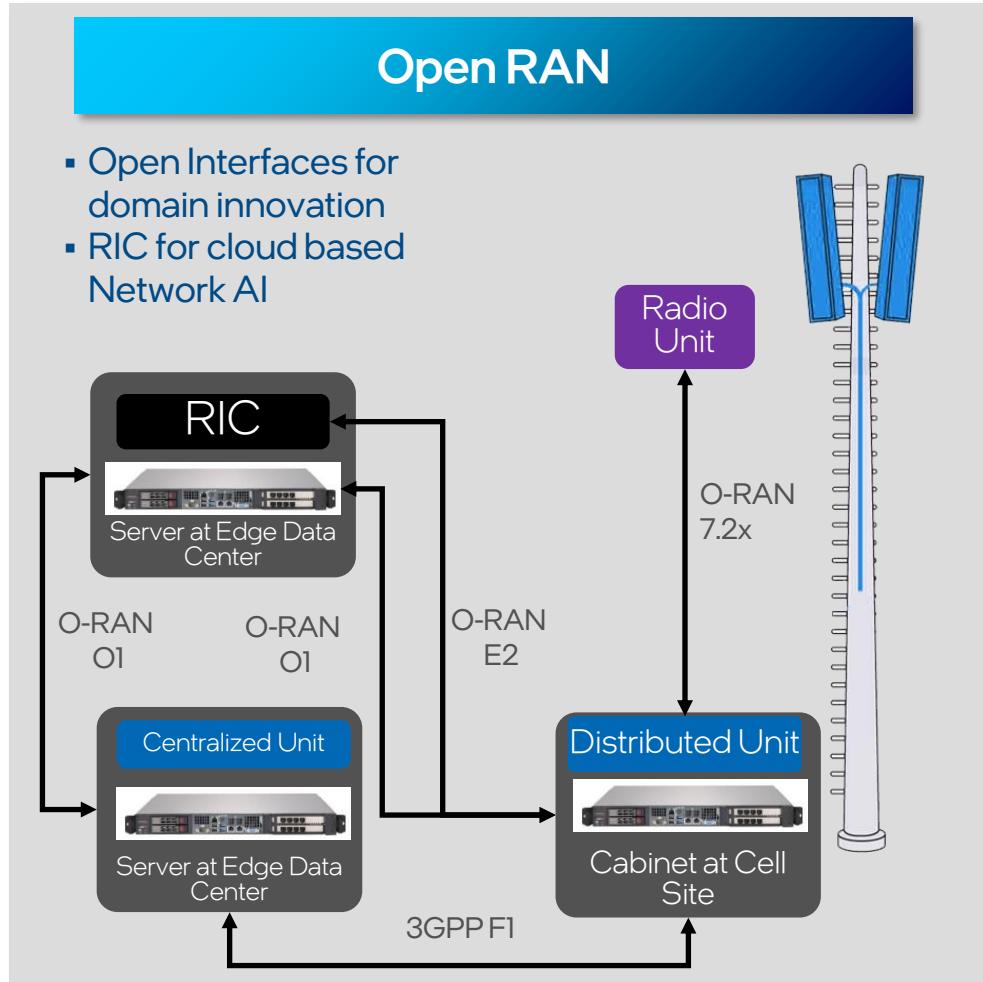
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# Forward Looking Statements Disclaimer

- Statements in this presentation that refer to future plans or expectations are forward-looking statements. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at [www.intc.com](http://www.intc.com).

# Overview

# vRAN / CloudRAN / OpenRAN Transition & Why



CloudRAN is vRAN but may have proprietary i/f w/single vendor  
OpenRAN is vRAN but has Open I/F interoperability

## Benefits

- Vendor interoperability & optionality allows for best of breed configurations
- Enablement of flexibility and agility for operator deployments
- Common Cloud Native SW platform from Core to Access to Edge
- Promises to increase the pace of innovation for Telco community

# vRAN / OpenRAN is Becoming Mainstream

## Operators

**verizon**



**dish**

**Rakuten**



**KDDI**



## Vendors



**ERICSSON**

**Rakuten Symphony**

**SAMSUNG**

**MAVENIR™**

 **Parallel  
WIRELESS**

**CORNING**

## Analysts

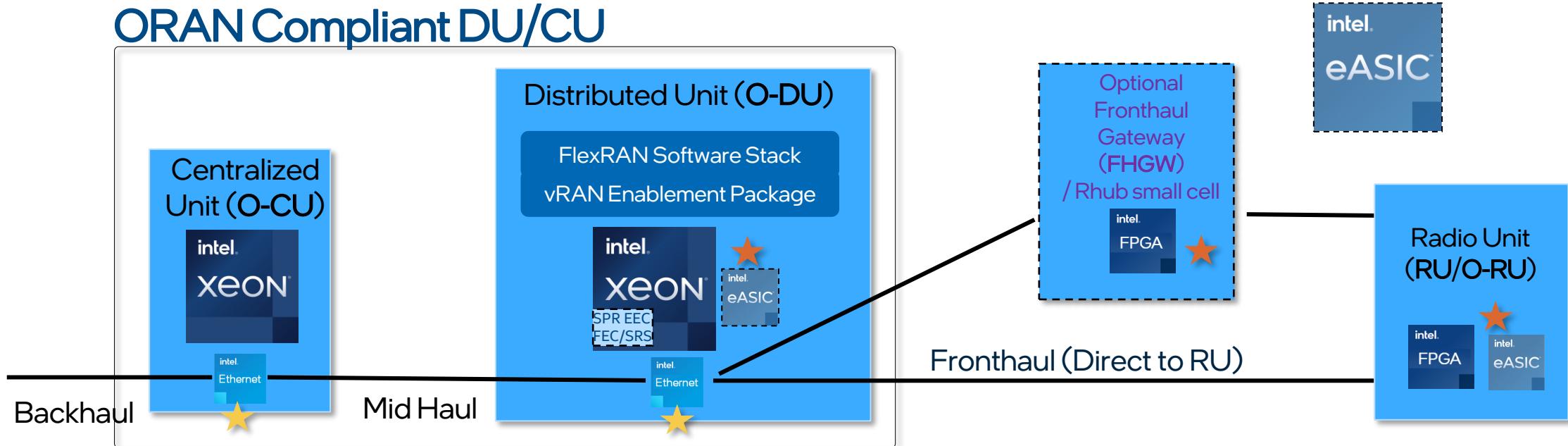
**Dell'Oro bumps revenue forecast 50% as open RAN gains steam**

By Diana Goovaerts • Sep 3, 2021 09:07am

Dell'Oro has released its latest open RAN report, which, according to preliminary findings, forecasts that the nascent tech will account for around 15% of the overall 2G-5G RAN market by 2026.

# Building Blocks for the RAN: O-DU/CU, FHGW, Radio

## ORAN Compliant DU/CU



FlexRAN™ Architecture (HW and SW) enables the **end-to-end** Open RAN solutions with **Intel® Xeon®**, **Intel® FPGA**, **Intel® eASIC™** and **Intel® Ethernet** technologies

★ CPU is the Main Processing Block

★ Ethernet for Connectivity (BH, MH, FH-eCPRI/SyncE/1588 direct RU attach)

★ FPGA / eASIC for limited RAN acceleration (e.g. FEC) or Lower L1 FH or for Radio

# Intel vRAN R&D: Enabling an Si Arch agnostic Cloud RAN

## FlexRAN™ SW

Source Code Released under Intel® architecture license free of charge

### FlexRAN SW Consumption Models



Usecase 1: baseline for stack which is added to, enabling commercial RAN on Intel® architecture only



Usecase 2: consume some modules to augment own IP

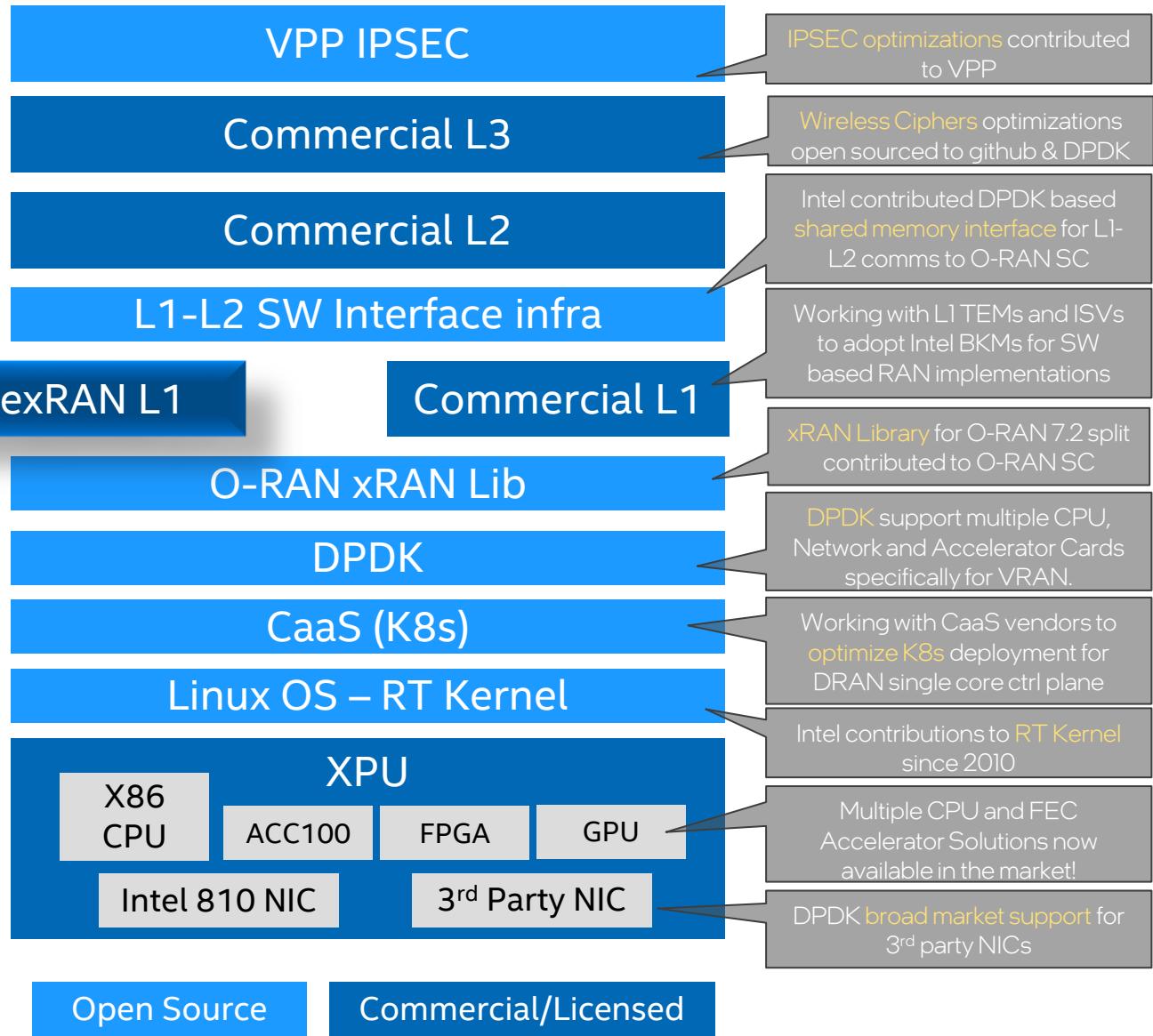


Usecase 3: benchmarking only no SW use

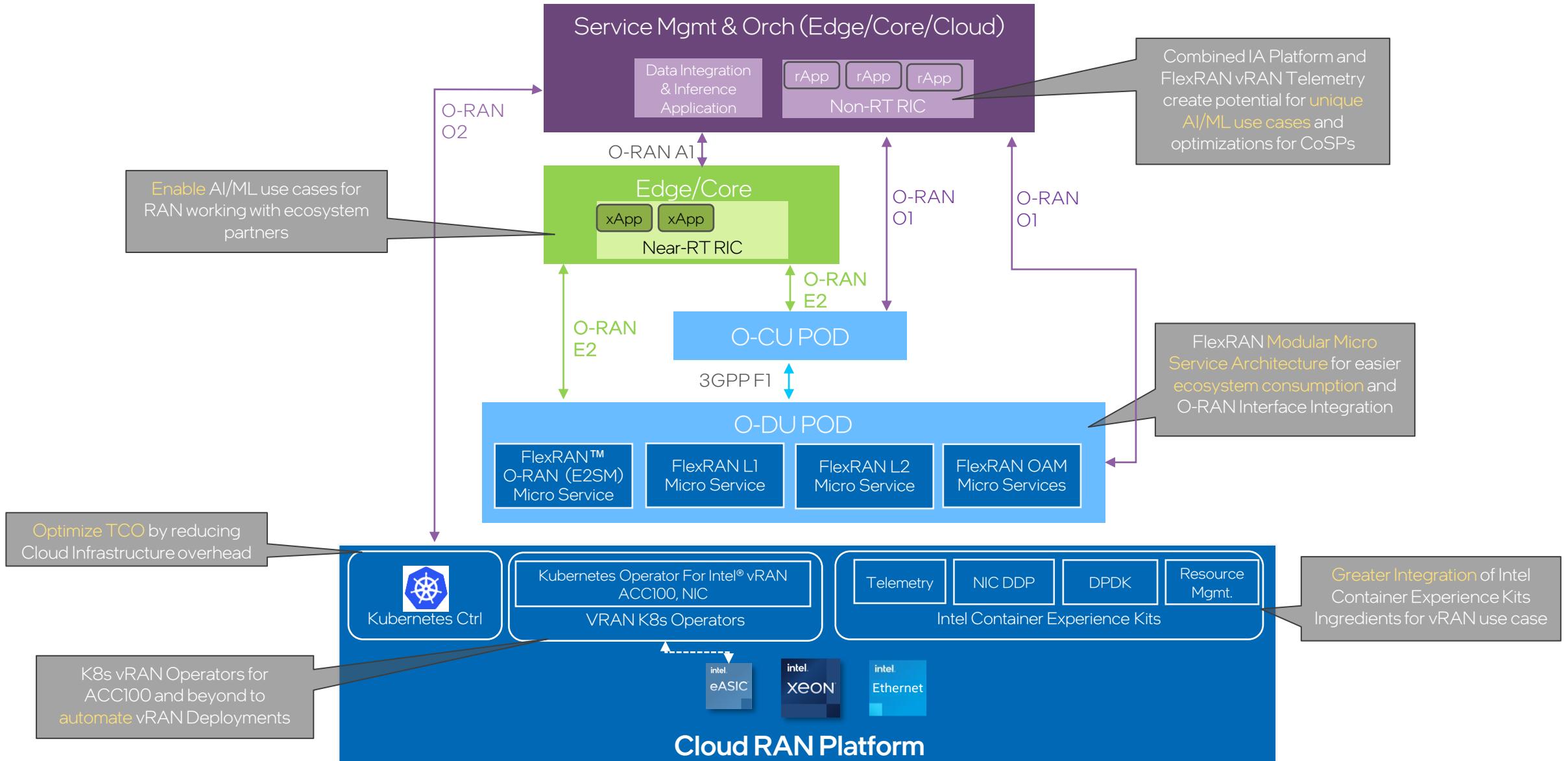


Ecosystem – vRAN Ecosystem consumes all BKMIs for developing a SW Based vRAN Solution

- HW OEMs
- System Integrators
- O-RU Integrations
- C/C++ Software Development Optimizations and ISA abstraction
- HW / SW Abstraction
- ISA/Cache/Memory etc..



# Cloud Native Architecture Goals

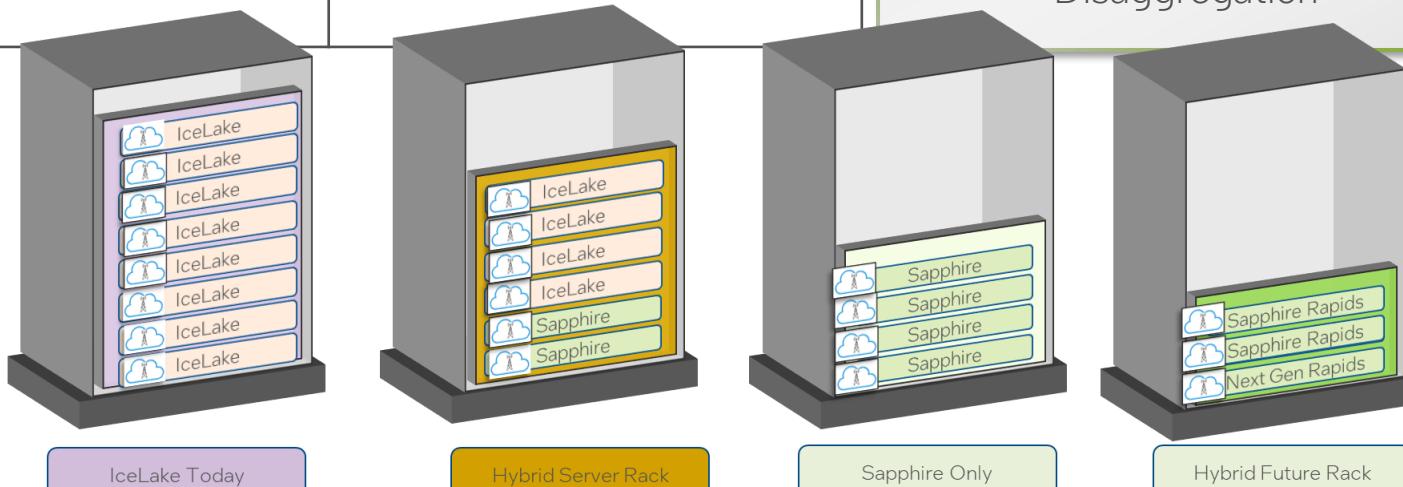


# Innovation

# Intel® C++ Class & C++ Standard Libraries for High Performant & Portable Code

	Intrinsic	Intel C++ Class Libraries (Dvec.h)
Complexity	Medium	Low
Portability	Medium	Medium
Performance	High	High
Run time uArch target		Intel® AVX-512 to 5GISA run time swap
Example	<pre>#include &lt;xmmmintrin.h&gt; __m128 a,b,c; a = _mm_add_ps(b,c);</pre>	<pre>#include &lt;dvec.h&gt; T &lt;type&gt; a,b,c; a = b + c;</pre>

- Intel C++ Class libraries allow developers to simplify code development and evolution, increase forward and backward portability and decrease maintenance costs
- Intel FlexRAN™ 22.03 (FlexRAN's first major Dvec release) delivered
  - Up to 85% reduction in source code
  - Up 7%-11% decrease in clock cycles
  - A run time system enabling same binary run on multiple uArchitectures (AVX512 or AVX512+ 5GISA) delivering open RAN HW / SW Disaggregation

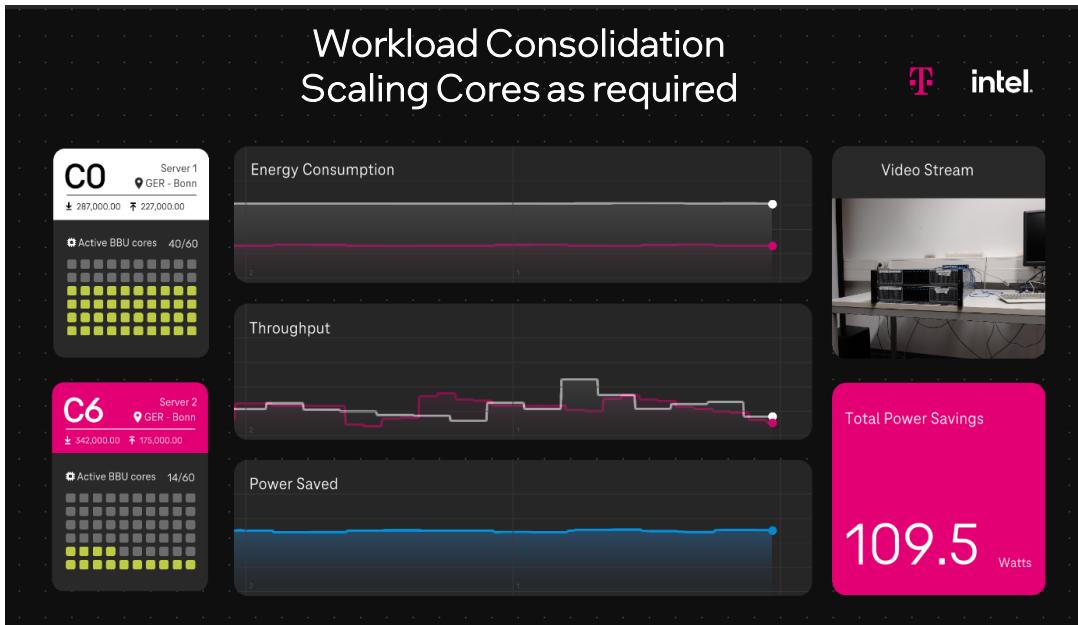


One SW Image: many CPU generations with any combination

[Intel® C++ Class Libraries](#)

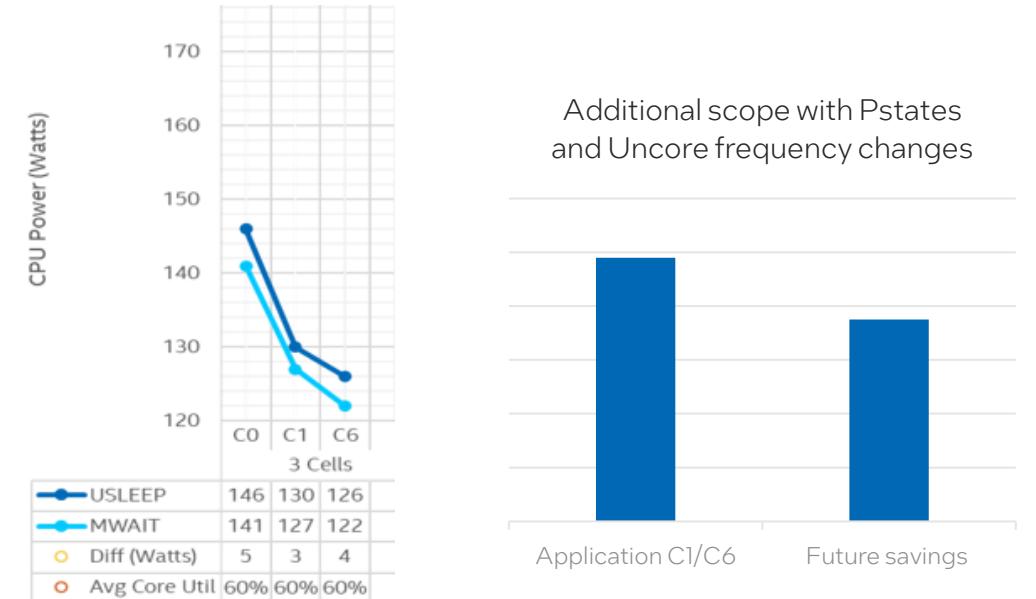
# vRAN Energy Efficiency

## Phase 1: Current Technologies MWC 2022 Demo with DTAG



Workload: 18 cells, 20 MHz 4x4 running on 40 cores compared to 14 cores on optimized server

## Phase 2 : Future Technologies in development



P-States to tailor CPU Freq to traffic throughput and reduce power consumption

Uncore reduce uncore frequency during periods of low traffic throughput

UMWAIT new family of "wait" instructions that give fine grain control over C1 state to application. Targeted for I/O polling threads

vRAN SW directly influence per core c-states for intelligent Cloud RAN Energy Efficiency

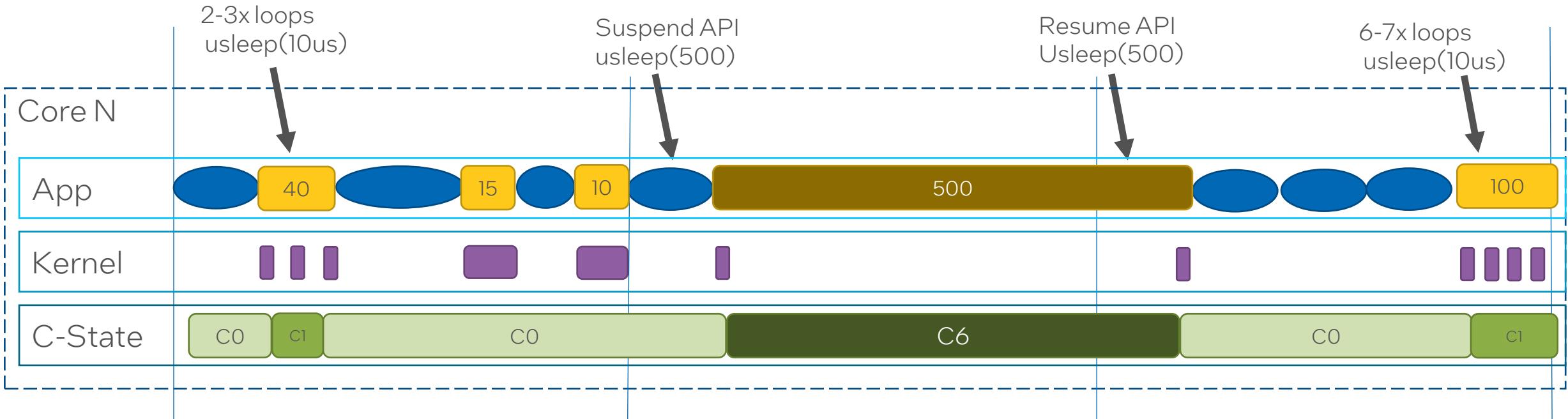
Platform ICX 6338N (185 Watt TDP)

Config Core 2.5GHz; Uncore 1.8Ghz; 8 DIMMs 16GB each

Intel/Ericsson CND: 4349934

# eBBU Scheduler Enhanced Dynamic Power Savings

- Just like any application, the L1 application has busy (*in blue*) and idle (*in yellow*) periods per TTI
- During these smaller idle periods, the scheduler does a continuous usleep(10) till it finds a task in the queue...OS puts in C0 state until task arrives in queue
- Predictive application logic per TTI using L1/L2 stats (RB util, BW, UE/TTI) for longer C6 sleep
- Suspend API coordinates HT pairs from pool to do usleep(500) ...OS puts in C6



# Small Cells

# Small Cells Success Story

[https://b2b.10086.cn/b2b/main/viewNoticeContent.html?noticeBean.id=874212&jump\\_from=1\\_05\\_37\\_01](https://b2b.10086.cn/b2b/main/viewNoticeContent.html?noticeBean.id=874212&jump_from=1_05_37_01)

 打印预览

## China Mobile's centralized procurement of expanded leather station equipment from 2022 to 2023\_Bid-winning candidate announcement

China Post and Telecommunications Equipment Group Co., Ltd. China Mobile's centralized procurement of expanded leather station equipment from 2022 to 2023 will open the bid at 2022-05-30 09:30, and complete the evaluation in accordance with the relevant national bidding laws and regulations and the bid evaluation method stated in the bidding documents.

The bid-winning candidates are now announced as follows:

### 1. Bidding quotations of the successful bidders and the situation of winning the bids:

Bidding Package 1 Single-mode Expanded Leather Station:

The 1st winning candidate: Comba Network System Co., Ltd, the bid price: 388725000.00 yuan (excluding tax), the winning share is 23.91%;

the 2nd winning candidate: Ruijie Networks Co., Ltd., bidding price: 405604500.00 yuan (excluding tax), the winning bid share is 19.57%;

the third winning candidate: Scitech Information Technology Co., Ltd, bidding price: 388600000.00 yuan (excluding tax), the winning bid share is 17.39%;

the 4th winning candidate: Lenovo (Beijing) Co., Ltd, the bid price: 390001230.00 yuan (excluding tax), the winning share is 15.22%;

the 5th bid winning candidate: Shenzhen Guoren Wireless Communication Co., Ltd, the bidding price: 402798375.00 Yuan (tax excluded), the winning bid share is 13.04%;

the sixth winning candidate: CITIC Mobile Communication Technology Co., Ltd, the bid price: 415402500.00 yuan (tax excluded), the winning bid share is 10.87%.

Bidding Package 2 Dual-mode Expanded Leather Station:

The 1st winning candidate: Comba Network System Co., Ltd, the bid price: 894375000.00 yuan (excluding tax), the winning share is 18.85%;

the 2nd winning candidate: CITIC Mobile Communication Technology Co., Ltd., bidding price: 923800000.00 yuan (excluding tax), the winning bid share is 15.94%;

No. 3 candidate for winning the bid: Scitech Information Technology Co., Ltd, bidding price: 819500000.00 yuan (excluding tax), winning the bid The share is 14.49%;

the fourth winning candidate: Shenzhen Guoren Wireless Communication Co., Ltd, the bidding price: 894070125.00 yuan (excluding tax), the winning share is 13.04%;

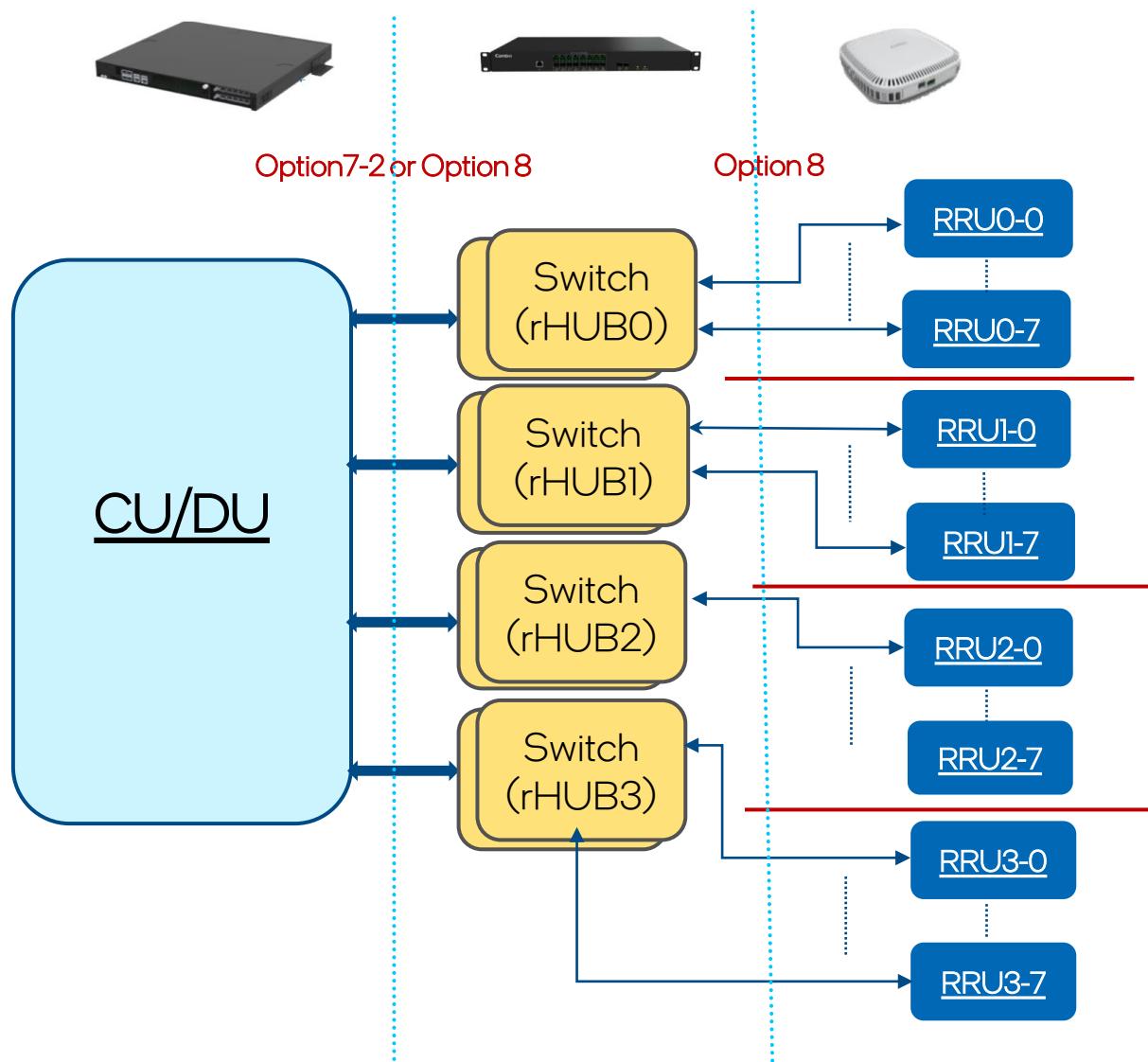
the fifth winning candidate: Lenovo (Beijing) Co., Ltd, the bidding price : 887488250.00 yuan (excluding tax), the winning bid share is 11.59%;

The sixth winning candidate: Xinhua Three Technology Co., Ltd, the bidding price: 1057899950.00 yuan (tax excluded), the winning bid share is 10.14%;

the seventh winning candidate: China Mobile Communications Group Design Institute Co., Ltd, the bidding price: 983435000.00 yuan ( excluding tax), the winning bid share is 8.70%;

the 8th bid winning candidate: Hangzhou Pingzhi Information Technology Co., Ltd, bidding price: 819454375.00 yuan (excluding tax), the winning bid share is 7.25%.

# Extended Picocell System Architecture



## Typical 3 types equipment

### DU:

Central Unit, L3/L2/L1 function rely on CU/DU Option

### rHub:

Switch device, L1/Switch function rely on CU/DU Option

### RRU:

Remote device, L1/Radio function rely on CU/DU Option

## System Topology

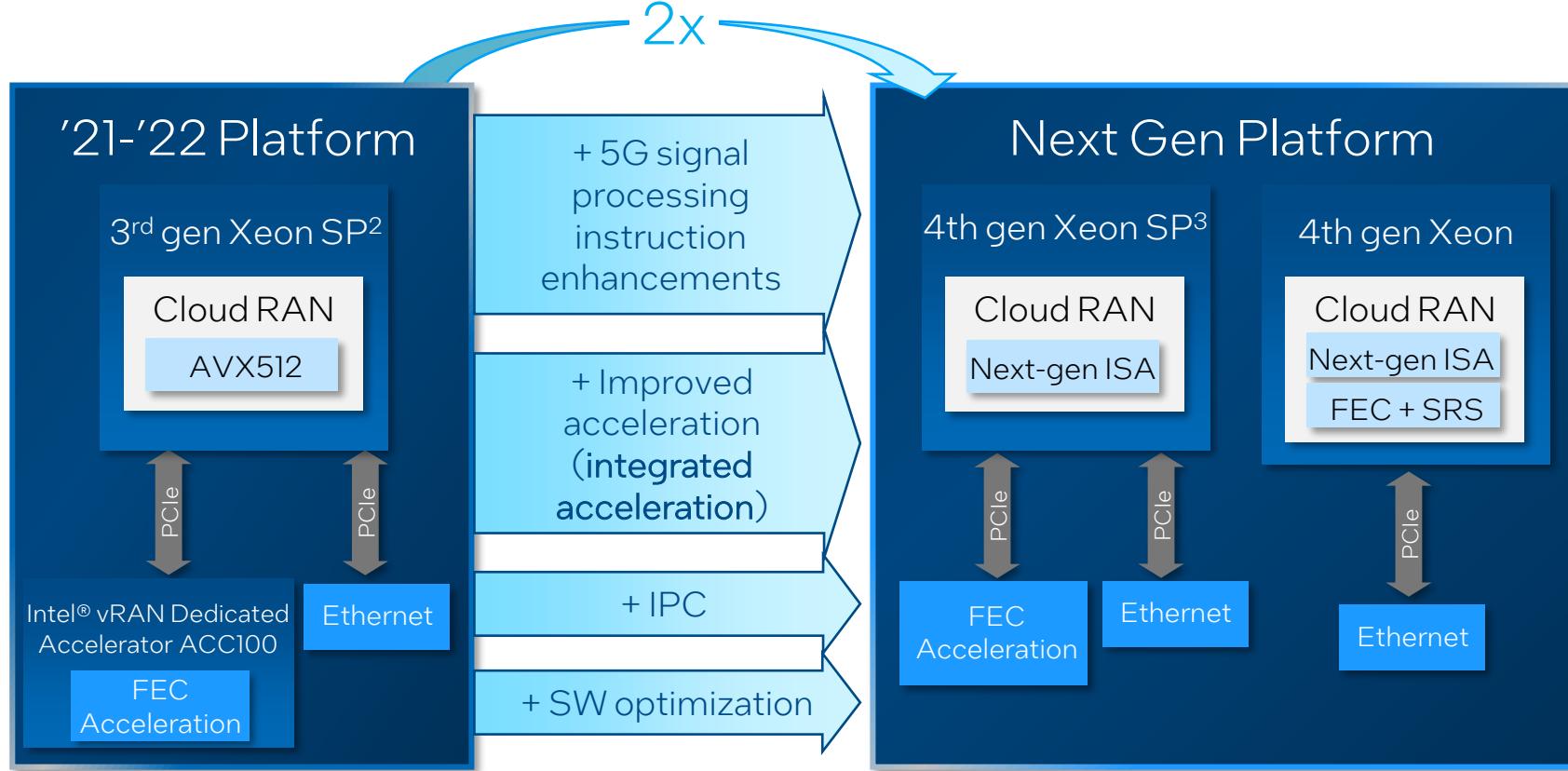
One DU support up to **4** rHUBs

Each rHUB support up to **8** RRUs

rHUB support 2-level cascading

# Roadmap

# Intel vRAN Solution – Up to 2X Capacity Gains<sup>1</sup>



Designed at SoC level for best performance, flexibility and software support

Next generation of Intel® Xeon® delivering up to 2x capacity per RAN site<sup>1</sup>

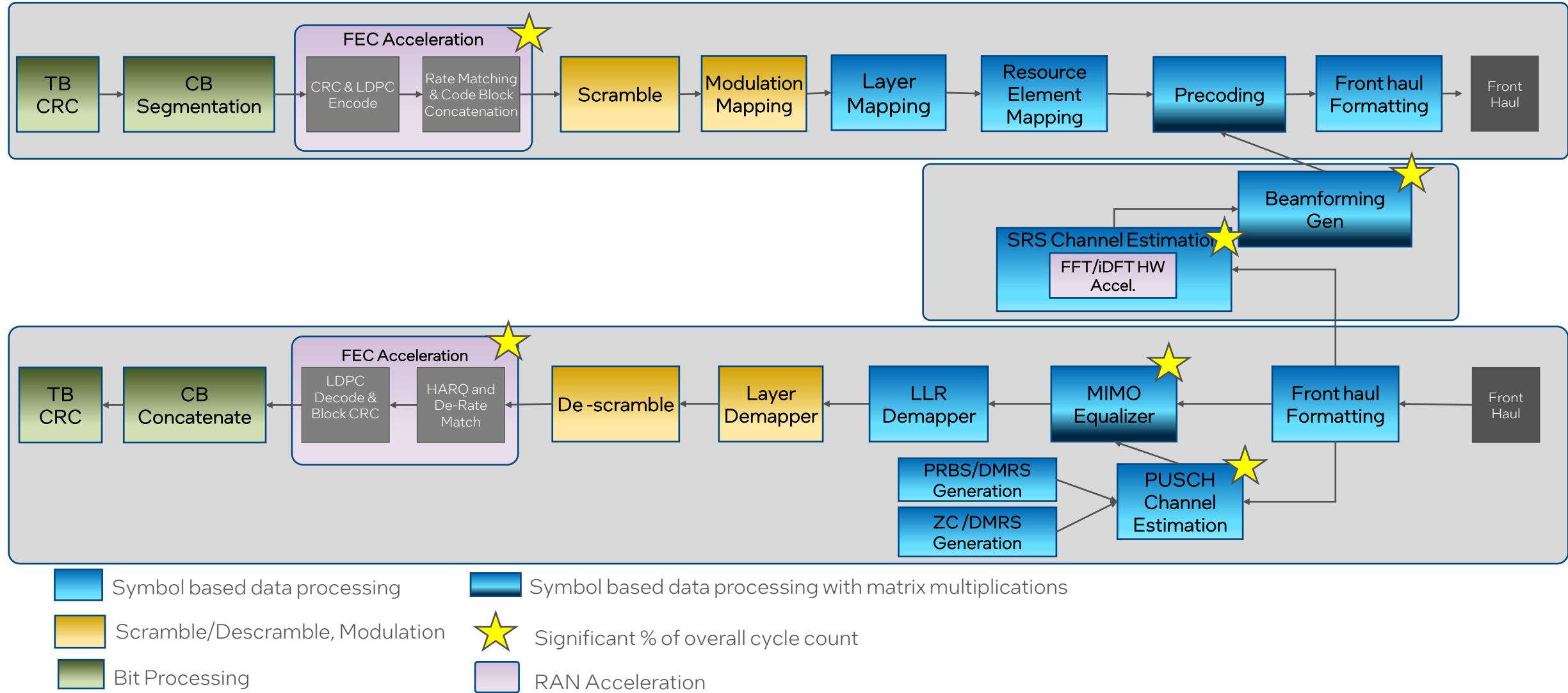
Supports high cell density and 64T64R Massive MIMO

<sup>1</sup> Claim estimated as of 2/10/2022 based on 4<sup>th</sup> generation Intel® Xeon® Scalable architecture improvements vs 3<sup>rd</sup> generation Intel® Xeon® Scalable at similar core counts on a test scenario using FlexRAN™ software. Results may vary.

Performance varies by use, configuration and other factors. Learn more at [www.intel.com/PerformanceIndex](http://www.intel.com/PerformanceIndex).

<sup>2</sup> 3rd gen Intel® Xeon® Scalable Processors, previously codenamed Ice Lake. <sup>3</sup> 4<sup>th</sup> gen Intel® Xeon® Scalable Processors, previously codenamed Sapphire Rapids.

# FlexRAN™ Pipeline – Next Gen RAN Acceleration for Massive MIMO



# Summary

# Questions?

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Join Us Next Time  
October 5<sup>th</sup> @ 8am PDT

Intel® Network Builders Insights Series  
Intel SOCs for MEC, Access and Security  
Infrastructure and Servers

Venkataraman Prasannan, Product Line Director, NECD, Intel



The Intel logo is displayed in white on a solid blue background. The word "intel" is written in a lowercase, sans-serif font. A small, solid blue square is positioned above the letter "i". The letter "i" has a vertical stroke on its left side. The letter "t" has a vertical stroke on its right side. The letter "e" has a vertical stroke on its left side. The letter "l" has a vertical stroke on its right side. A registered trademark symbol (®) is located at the bottom right of the "l".