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5G Hardware Acceleration with Intel® Agilex™ FPGA Based Silicom SmartNICs

Istvan Szonyi
VP of Engineering

Date: May 14, 2024
Time: 9AM PDT / 12PM EDT

intel network builders partner

5G Hardware Acceleration with Intel® Agilex™ FPGA Based Silicom SmartNICs

May 14,
9 am PT

Silicom Denmark A/S
FPGA SOLUTIONS

Istvan Szonyi

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Denmark A/S | FPGA Solutions

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Agenda

- Silicom Denmark - FPGA solutions
- Silicom FPGA SmartNIC solutions for 5G
- 5G HW acceleration
- TimeSync SmartNIC architecture
- N6011 Smart NIC with 5G vRAN use case
- 5G HW acceleration – FHM Use Case
- 5G HW acceleration – L1 SD-FEC Use Case
- N6011 SmartNIC – 5G HW acceleration benefits
- 400G Ethernet SmartNIC with HBM and PCIe Gen5
- Questions

Corporate Overview

Leading provider of **Data Center & Edge Computing** solutions for next generation Cloud, Telecom, Mobile Operator, Service Provider and On-Premise infrastructures

30+ years of experience delivering high performance NICs, Offload NICs (HW accelerators) and Smart FPGA-based NICS

Leading supplier of innovative Edge/CPE units to leading global Telcos and OEMs

Positioned to benefit from the growth of multiple rapidly-expanding markets:
SD-WAN, Cloud, Data Centers, 5G, NFV and Cyber Security

A public company NASDAQ(SILC)

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Silicom Denmark – FPGA solutions

FPGA R&D in Copenhagen, Denmark

with manufacturing facilities and Sales support organization too.

Long standing Intel® Partner Alliance Titanium tier member on with Intel® Altera® FPGA and SoC FPGA solutions

Strong SmartNIC portfolio with the latest Agilex™ 7 FPGA and SoC FPGA

Turn-key solutions with state-of-the-art HW, and integrated FPGA-SW applications

Optimizing vRAN with Intel® FPGA @ Brightalk in 2022

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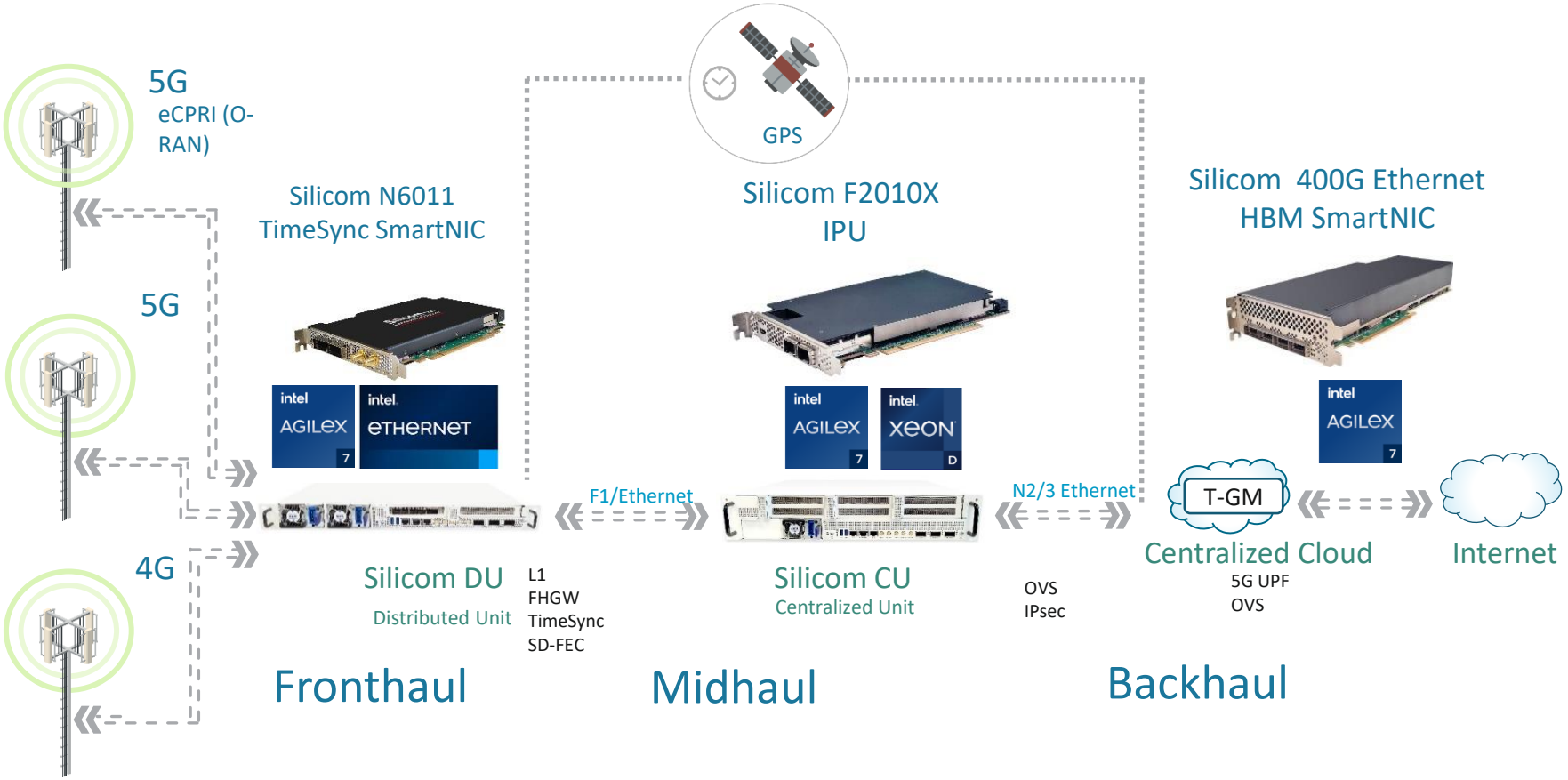
Silicom FPGA SmartNIC solution for 5G – from Edge to Cloud



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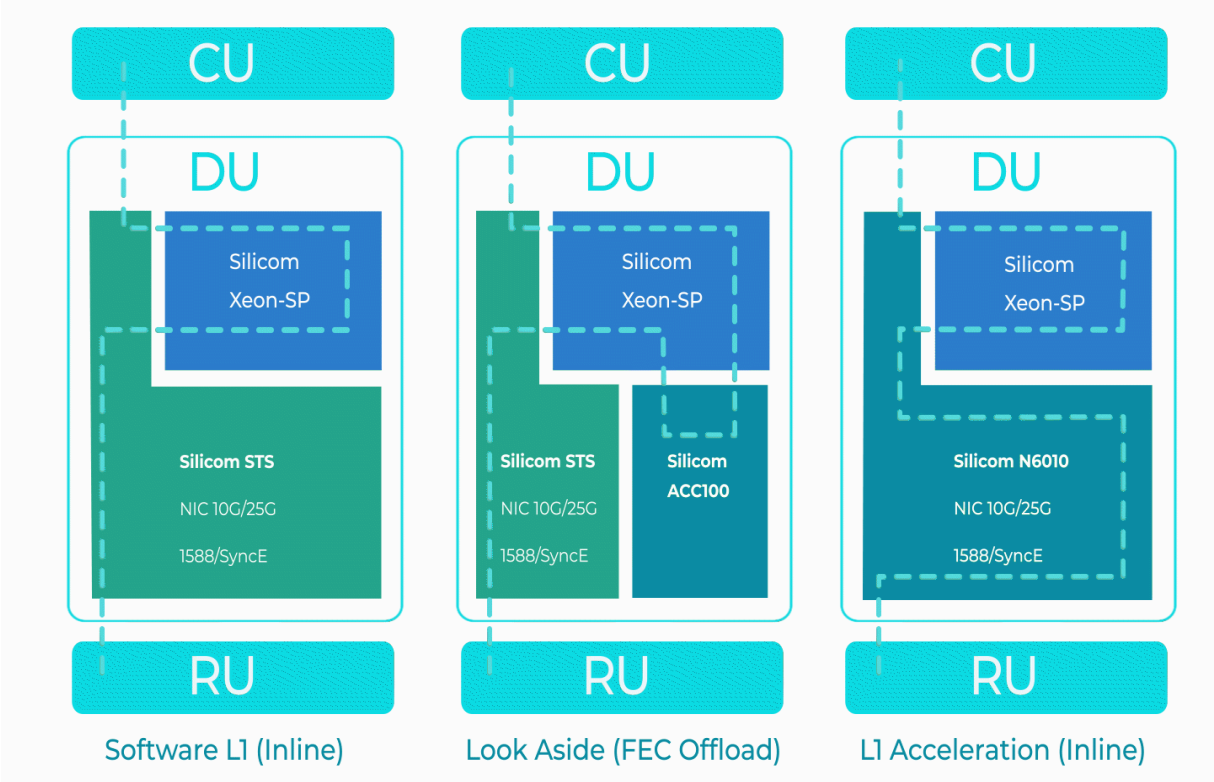
5G HW acceleration - L1 - SD-FEC



Silicom ACC100

+

Silicom STS NIC

Silicom N6010/11 SmartNIC

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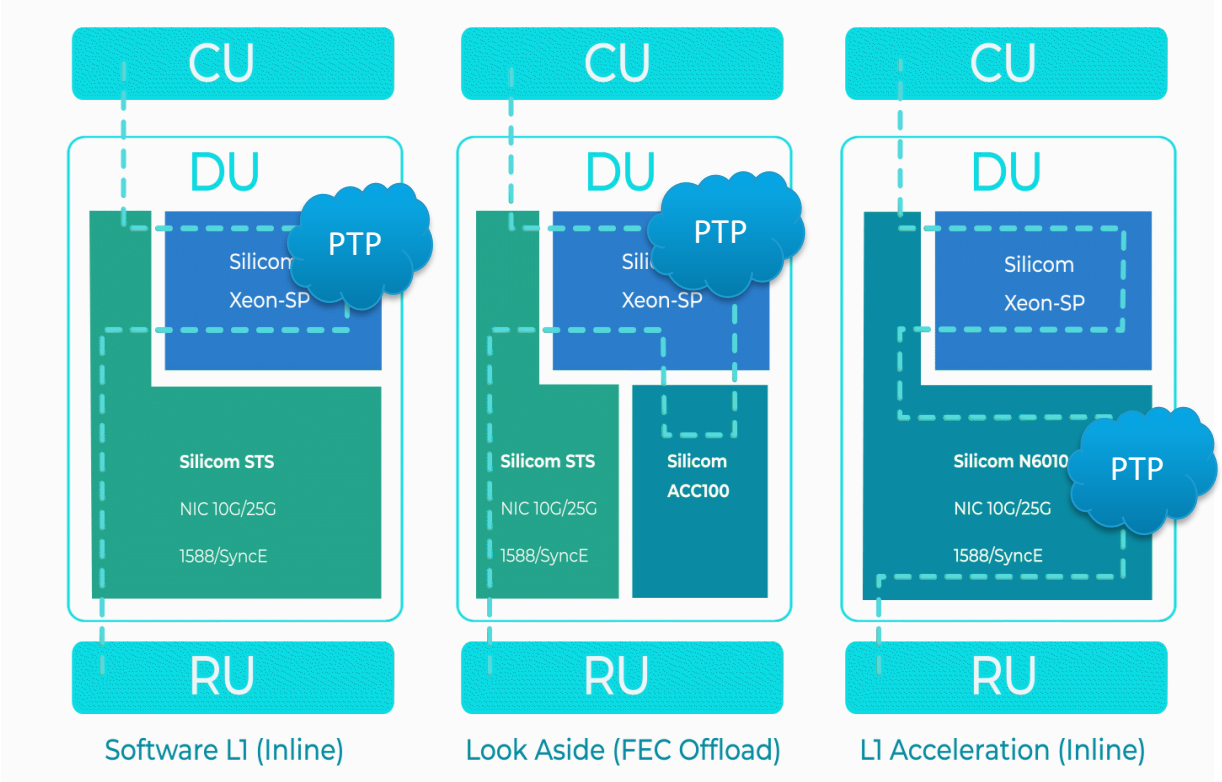
5G HW acceleration – L1 TimeSync



Silicom ACC100

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Silicom STS NIC

Silicom N6010/11 SmartNIC

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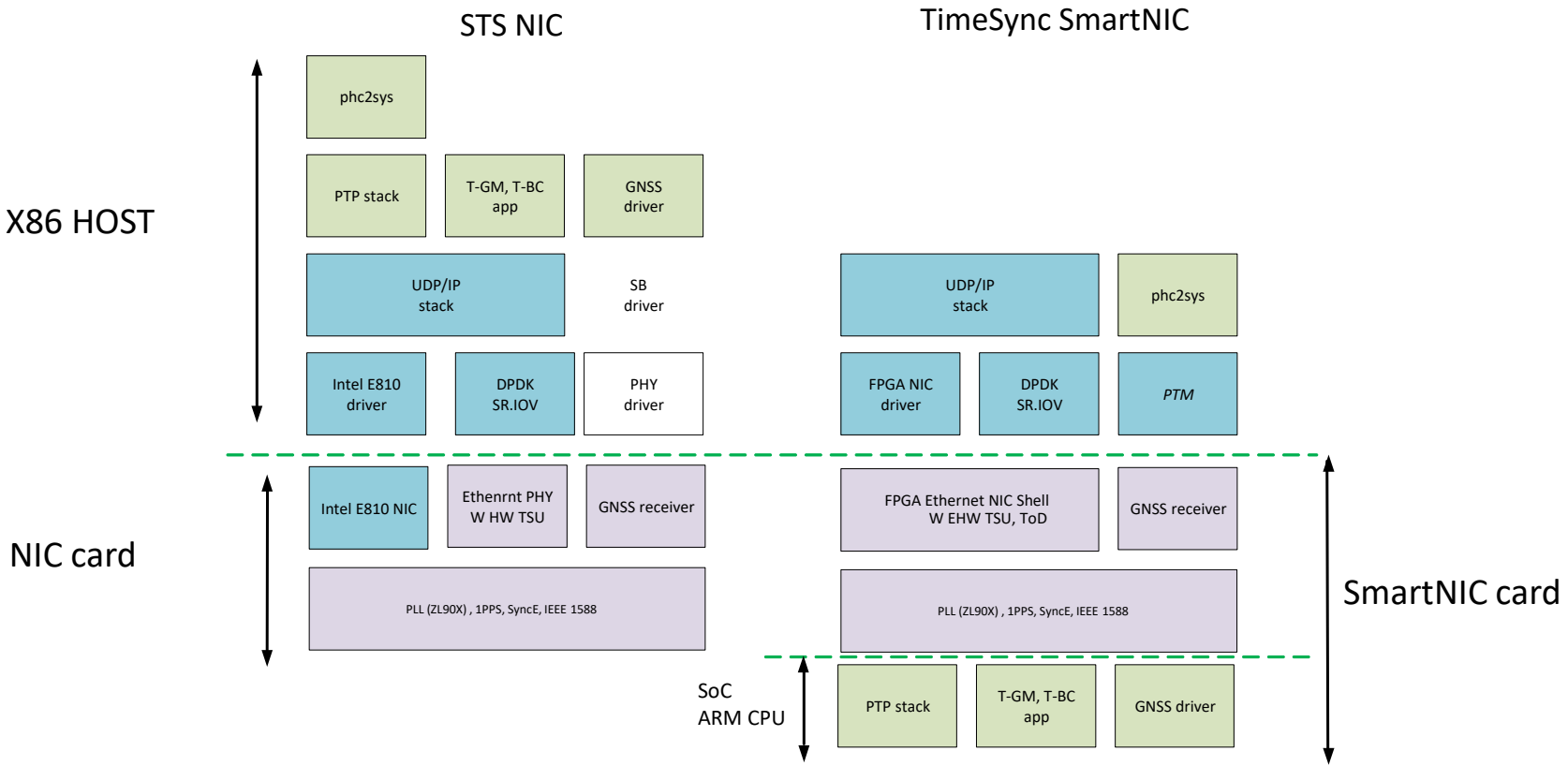
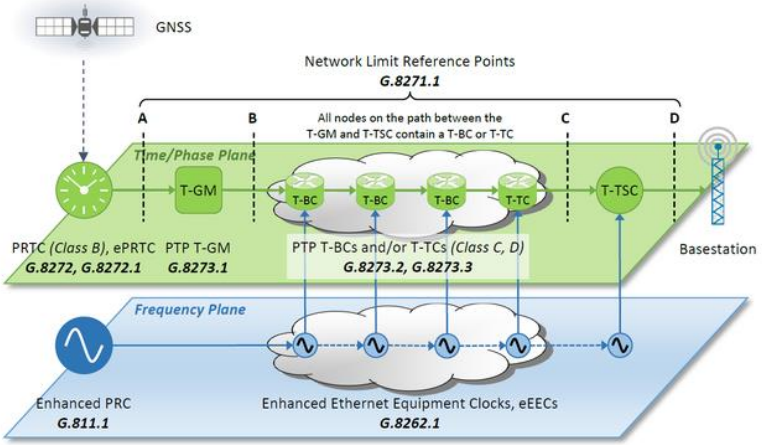
TimeSync SmartNIC architecture



Supported Time Synchronization Standards

- Support 1588/PTP over IPv4, IEEE1588v2
- Support SyncE /ITU-T G.8262
- T-BC/T-TSC Boundary and Slave Clock/G.8273.2
- T-GM Grand Master /G.8273.1 per G.8275.1 PTP Profile
- **Class C/D compliance on T-BC, T-TSC, SyncE!**
- Supported PTP stacks, running on FPGA SoC CPU(ARM):
  - ptp4l, the open source Linux PTP stack
  - zlsptp, proprietary PTP stack made from Microchip®
  - sptp, the open source Simple PTP developed at Meta used in large scale Data Centers
  - Intel® Precision Time Protocol Servo (Intel® PTP Servo)
  - phc2sys for HOST RTC synchronization with *PTM support*
- Supported OCXOs from: Vectron, Microchip, Rakon.



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N6011 5G vRAN use case

Silicom FPGA SmartNIC N6010/1 Platform with 5G vRAN workload (FEC + xHaul); single PCIe Gen4 x16 slot:

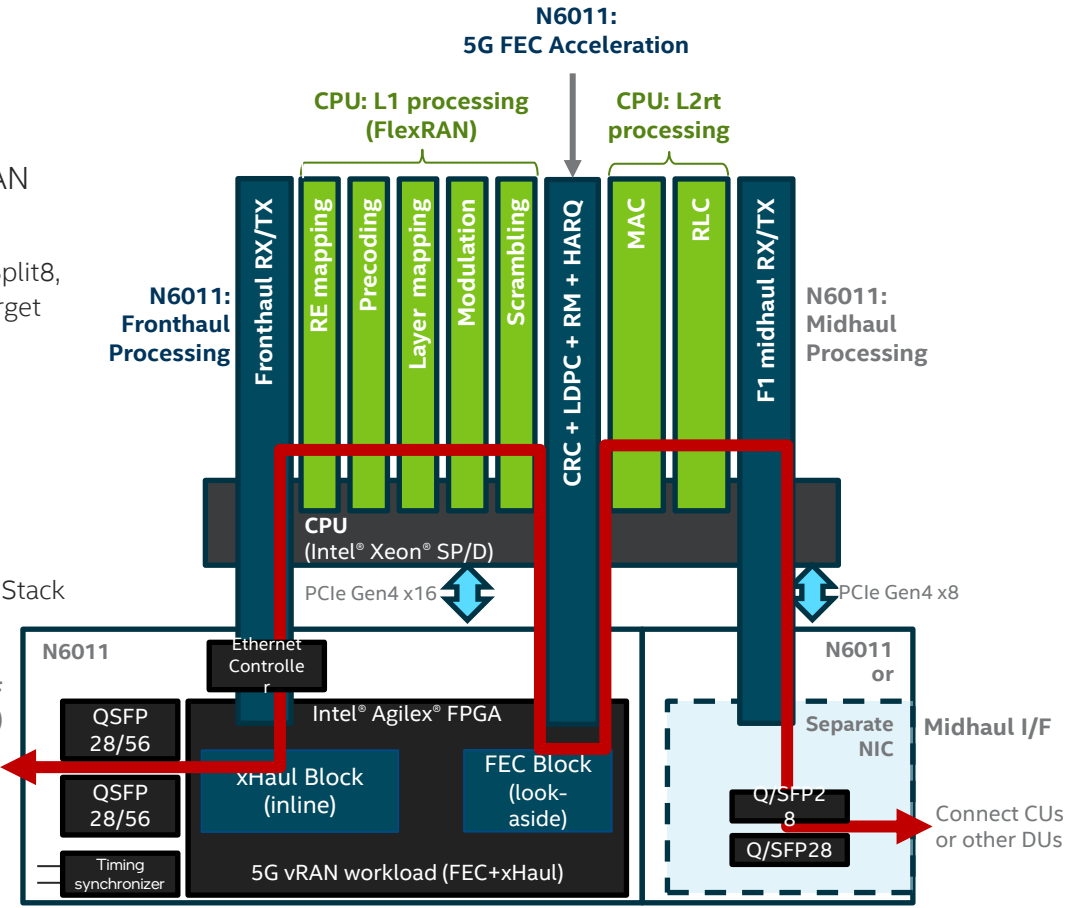
1. Fronthaul I/F: 8x10GE, 2x2x25GEs, 2x100GEs, Split 7-2x or Split8, O-RAN C3, C2 and C1 Timing Configuration (1588 GM/BC, target <3ns accuracy), CPRI support, SyncE
2. FEC processing: LDPC Gen 3.0 (URLLC support) encoder and decoder, Rate Match, De-Rate Match, HARQ, CRC, TB-CB conversion

3rd Gen Intel® Xeon® Scalable Processors

- L1 and L2rt functions in software (Intel® FlexRAN™ Reference Stack or customer's own)

vRAN use case example*:

- 24-36 cells 4T4R 20MHz, FDD, Narrow Band
- 3-6 cells 64T64R 100MHz, TDD, MidBand, mMIMO
- DRAN, CRAN, Private RAN



5G vDU use case (L1 + L2rt) high level abstraction
Not all functions listed, different L1 splits may apply

** Performance varies depending on traffic model definition. See Performance Estimates slide in Appendix*

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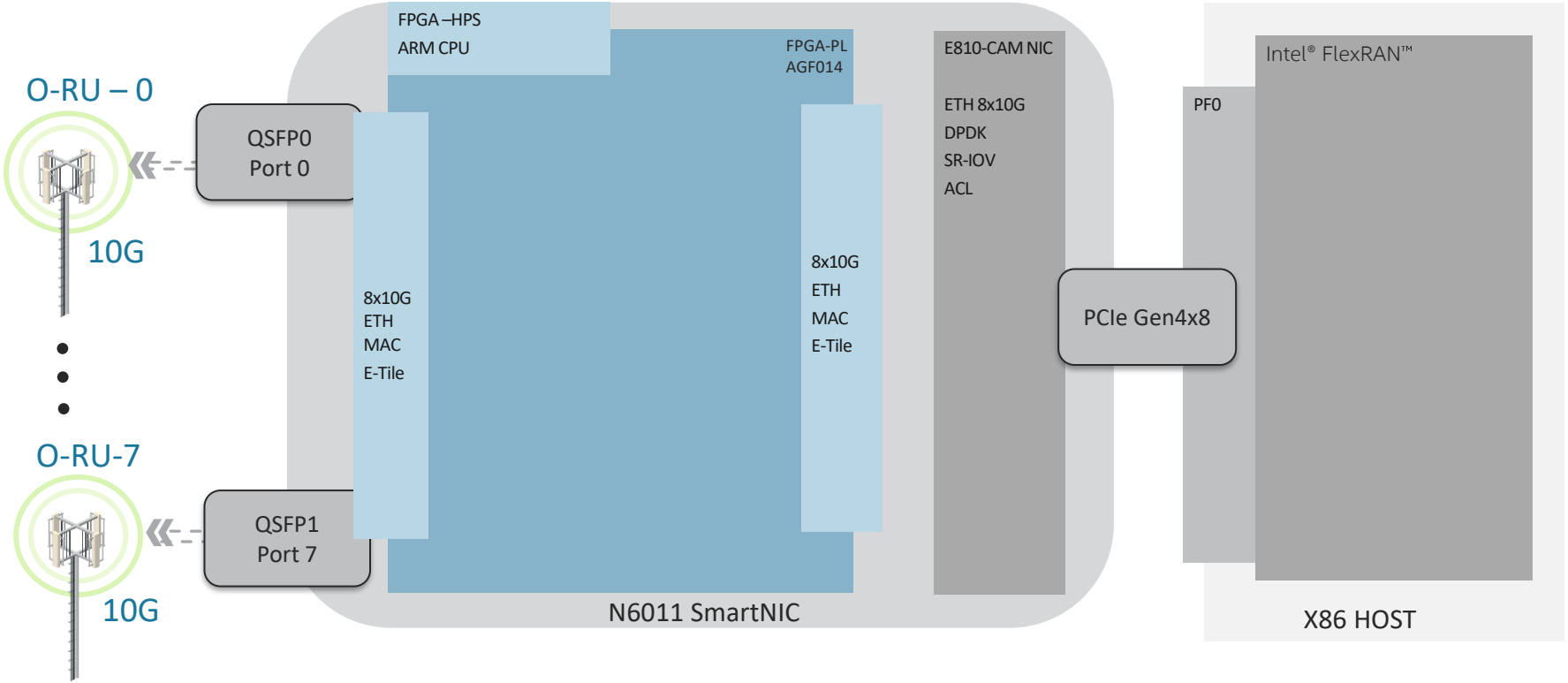
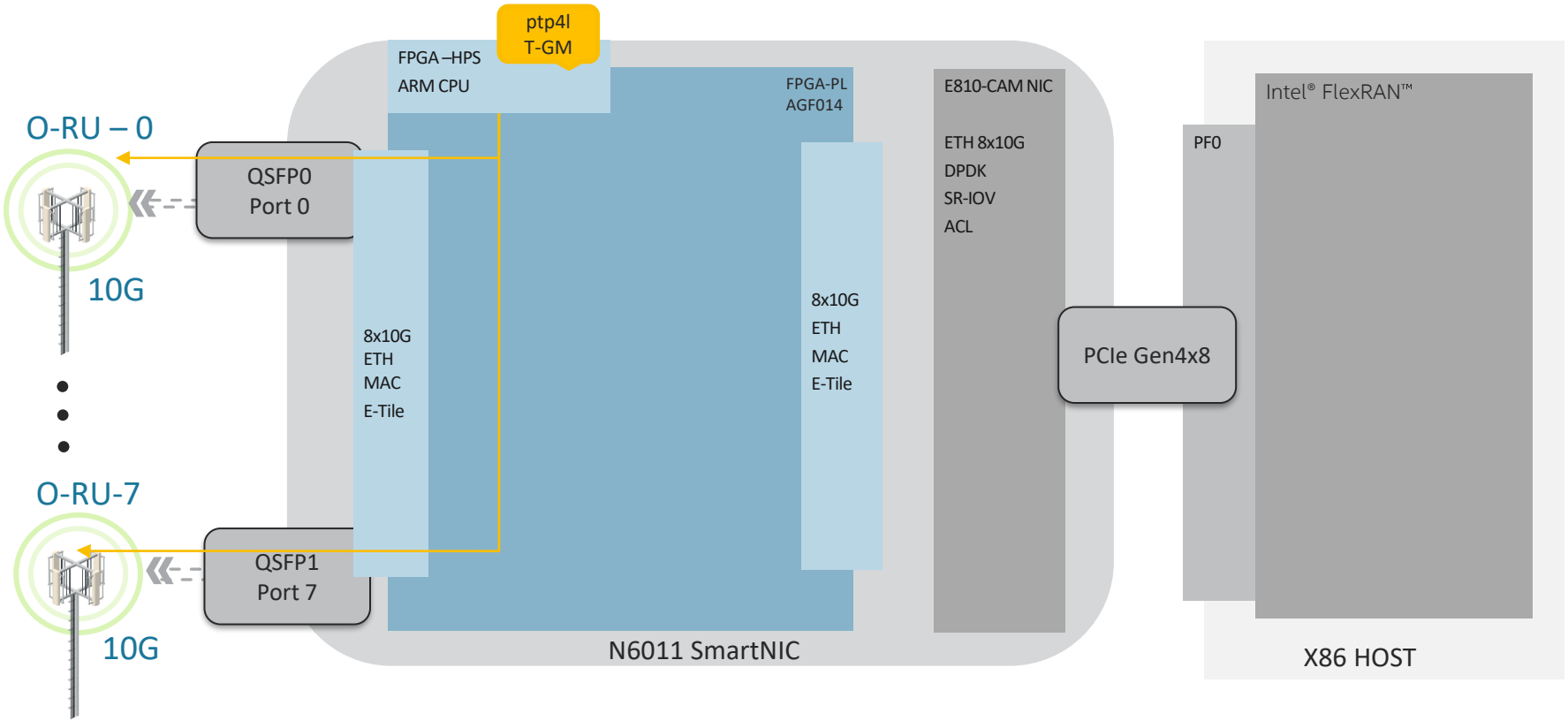
5G HW acceleration – FHM Use Case



5G HW acceleration – FHM Use Case



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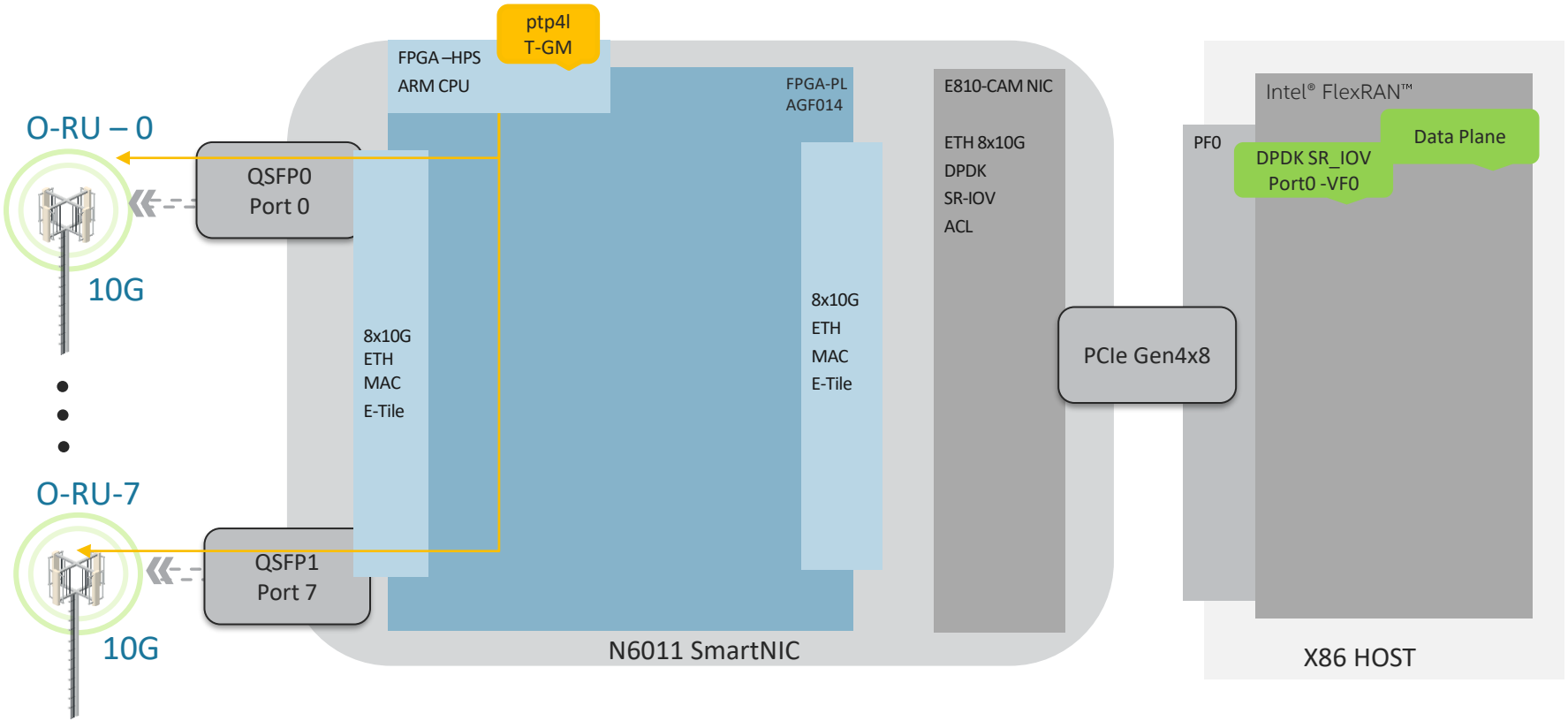
5G HW acceleration – FHM Use Case



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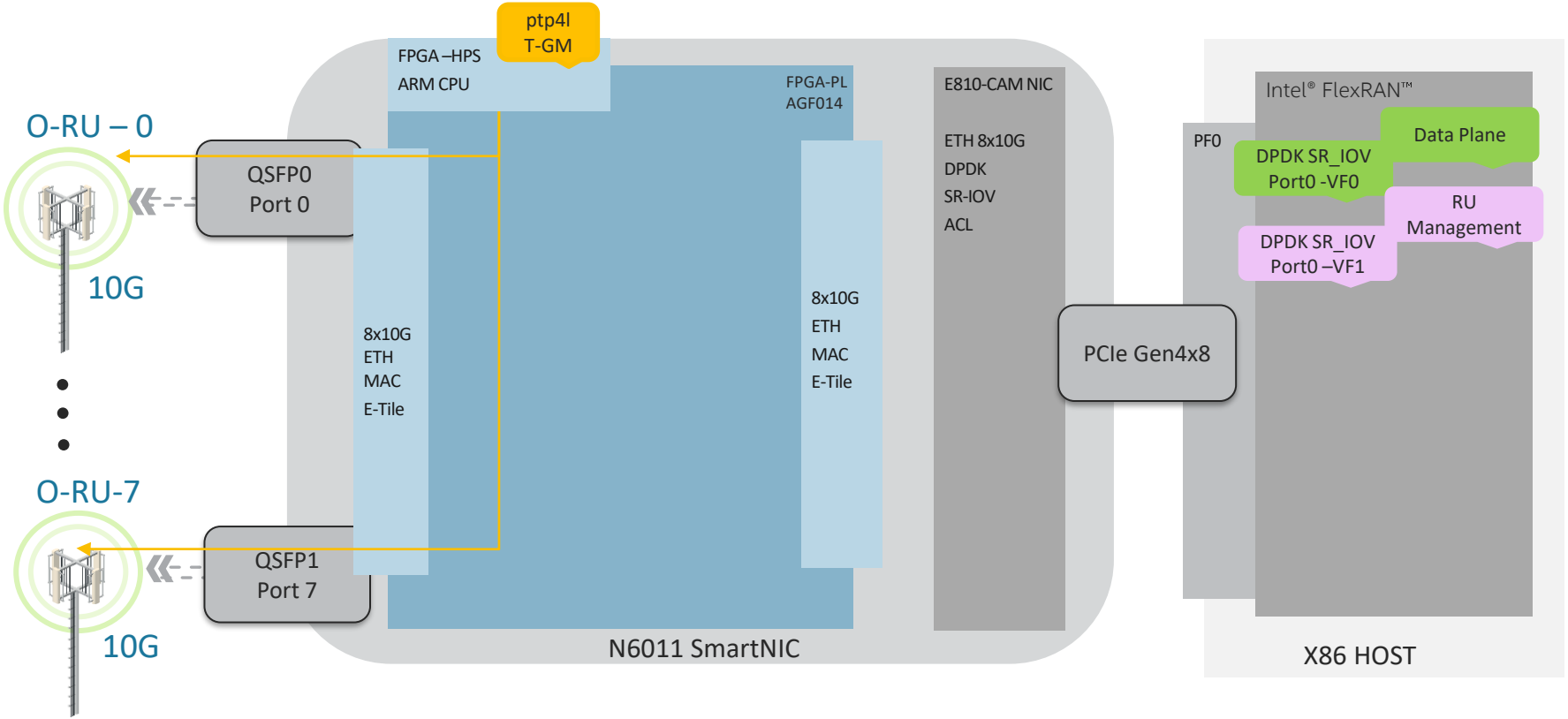

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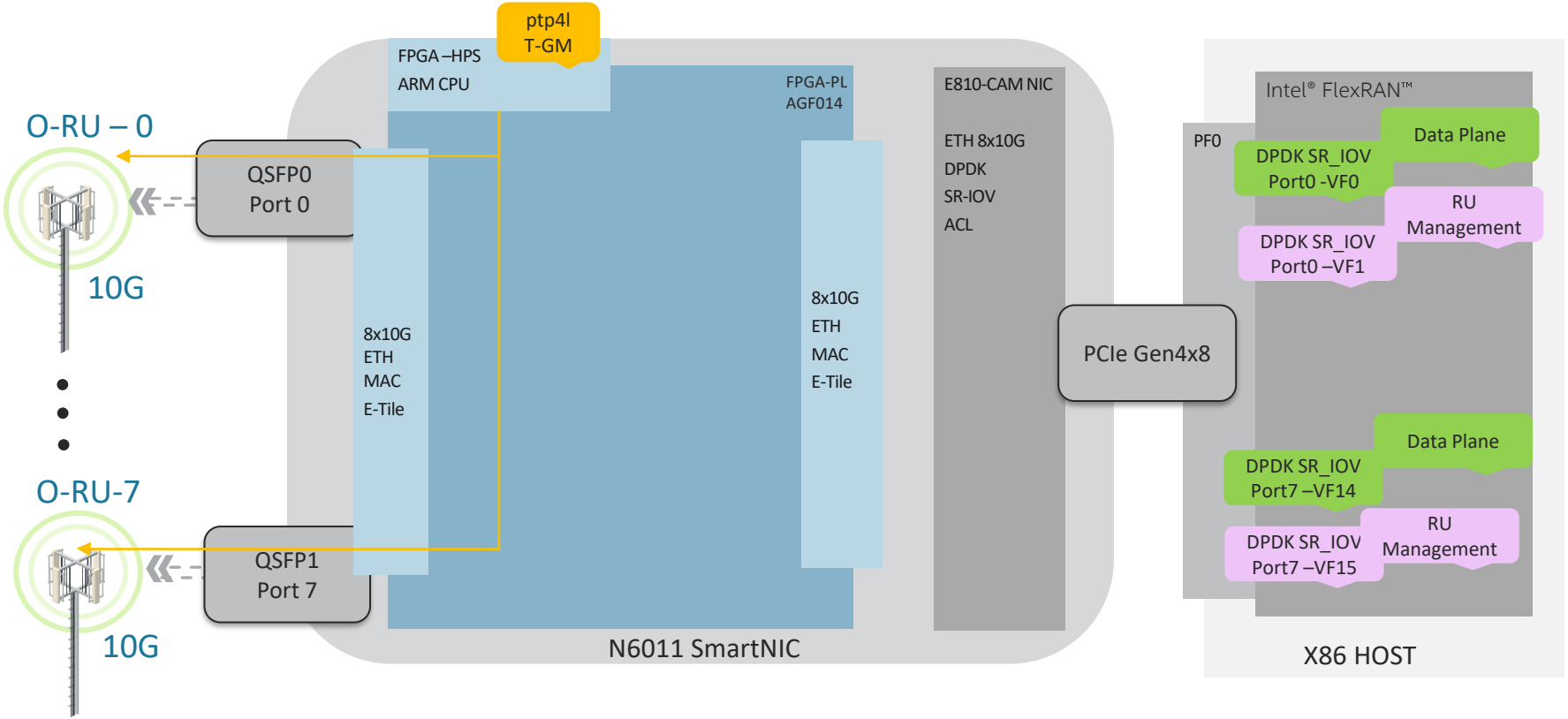

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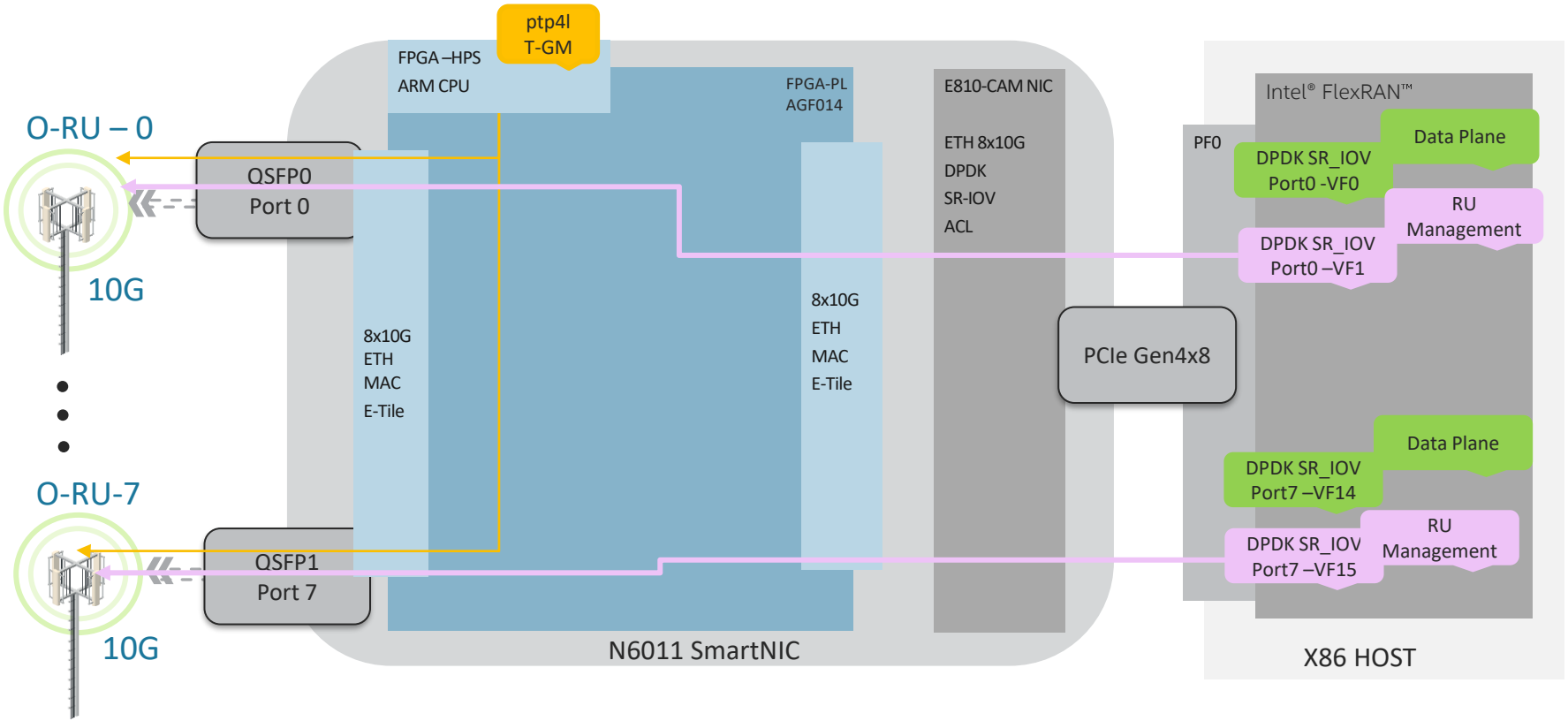

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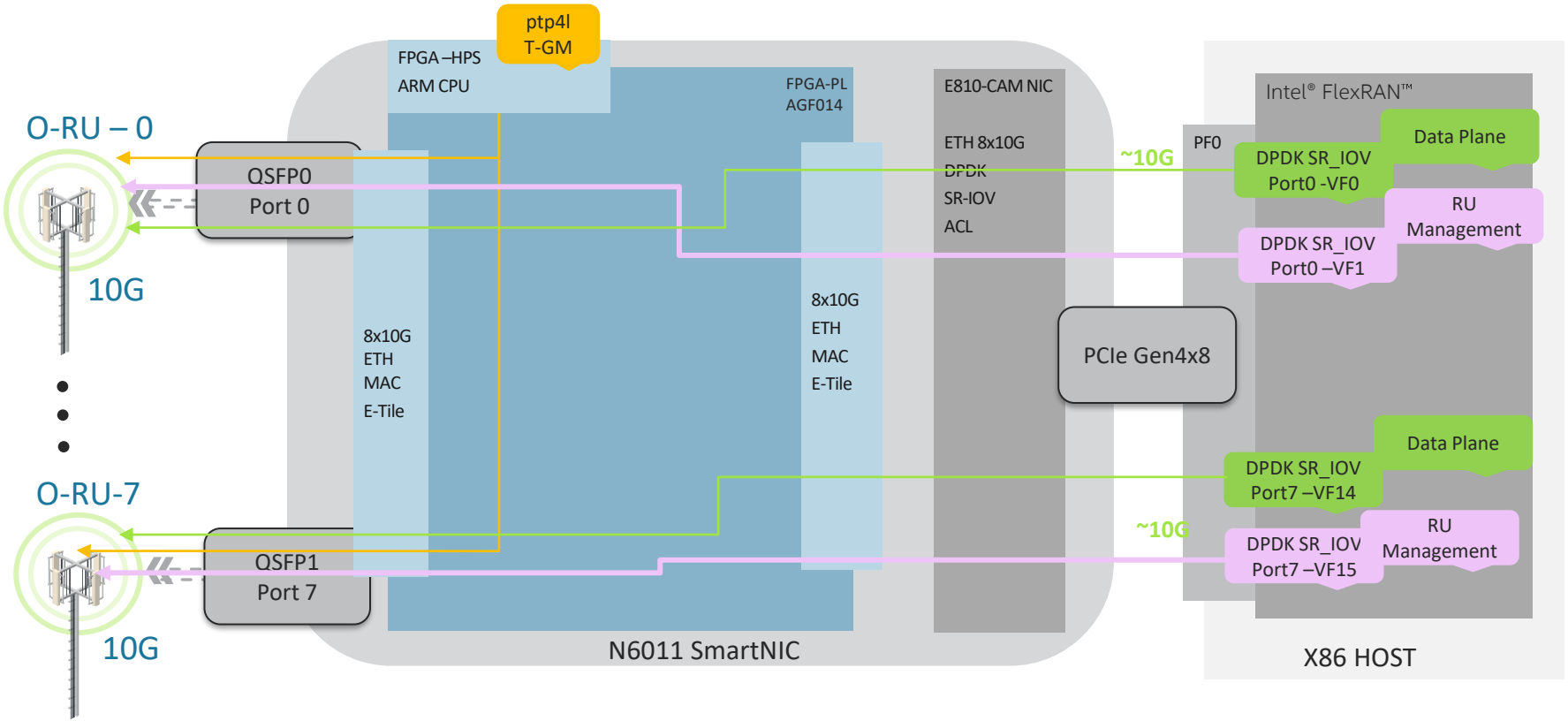
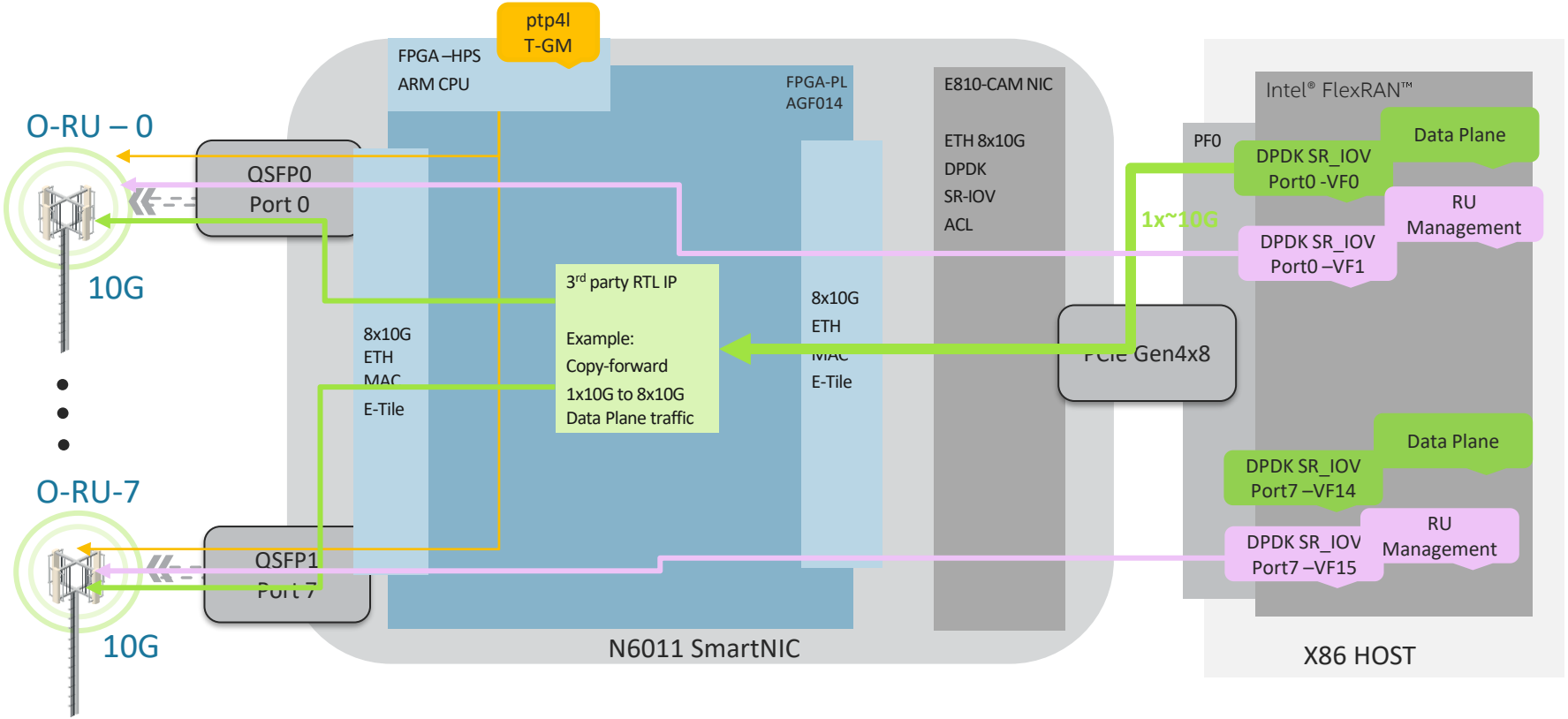


5G HW acceleration – FHM Use Case



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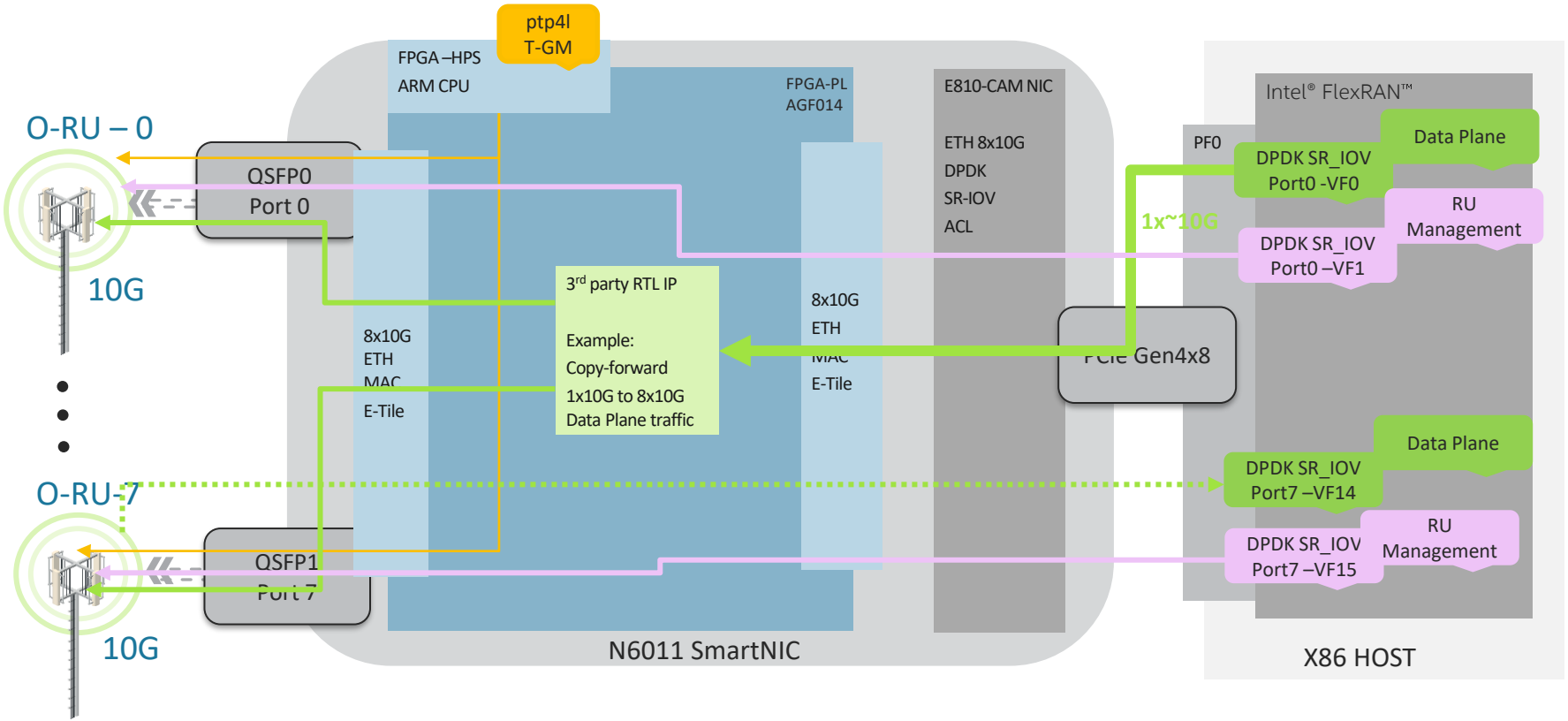
5G HW acceleration – FHM Use Case



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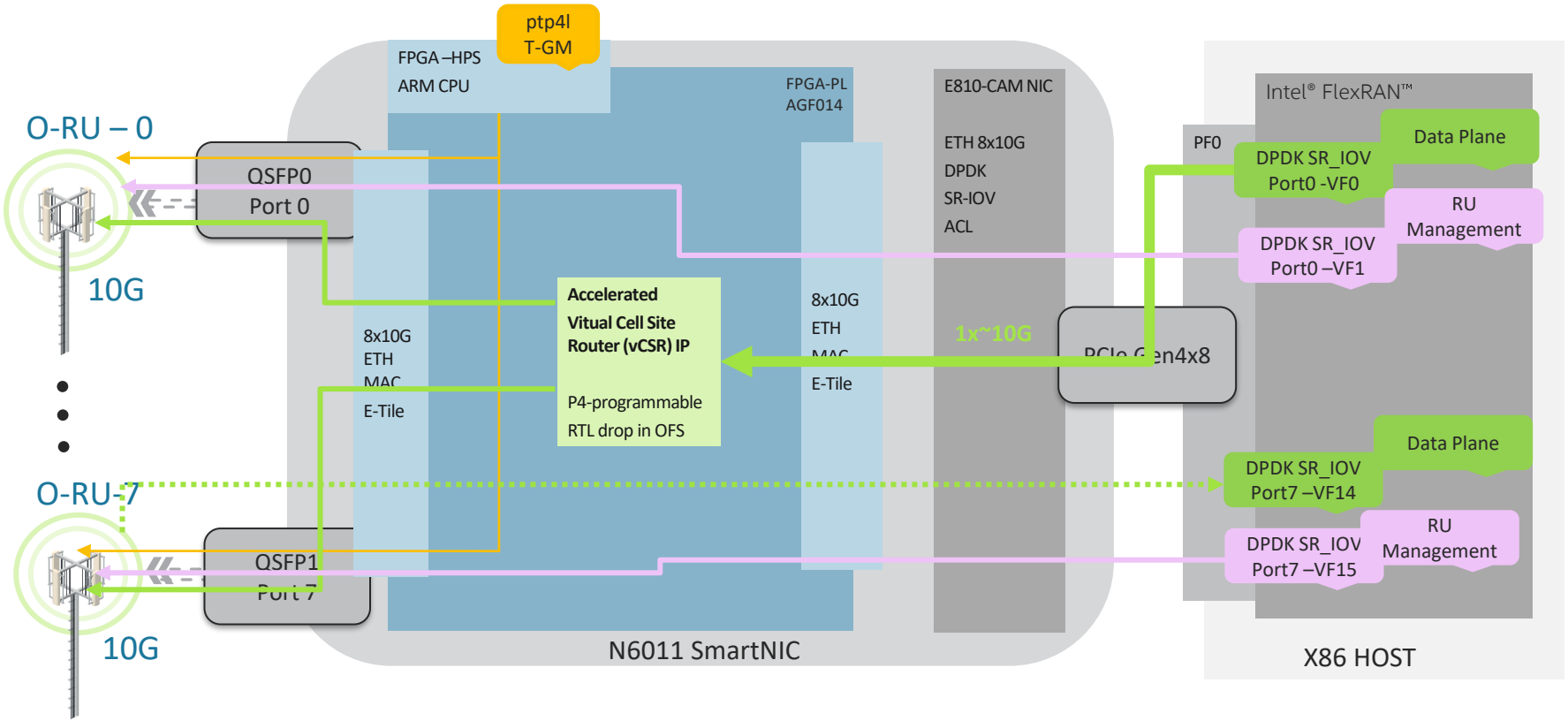
5G HW acceleration – FHM Use Case



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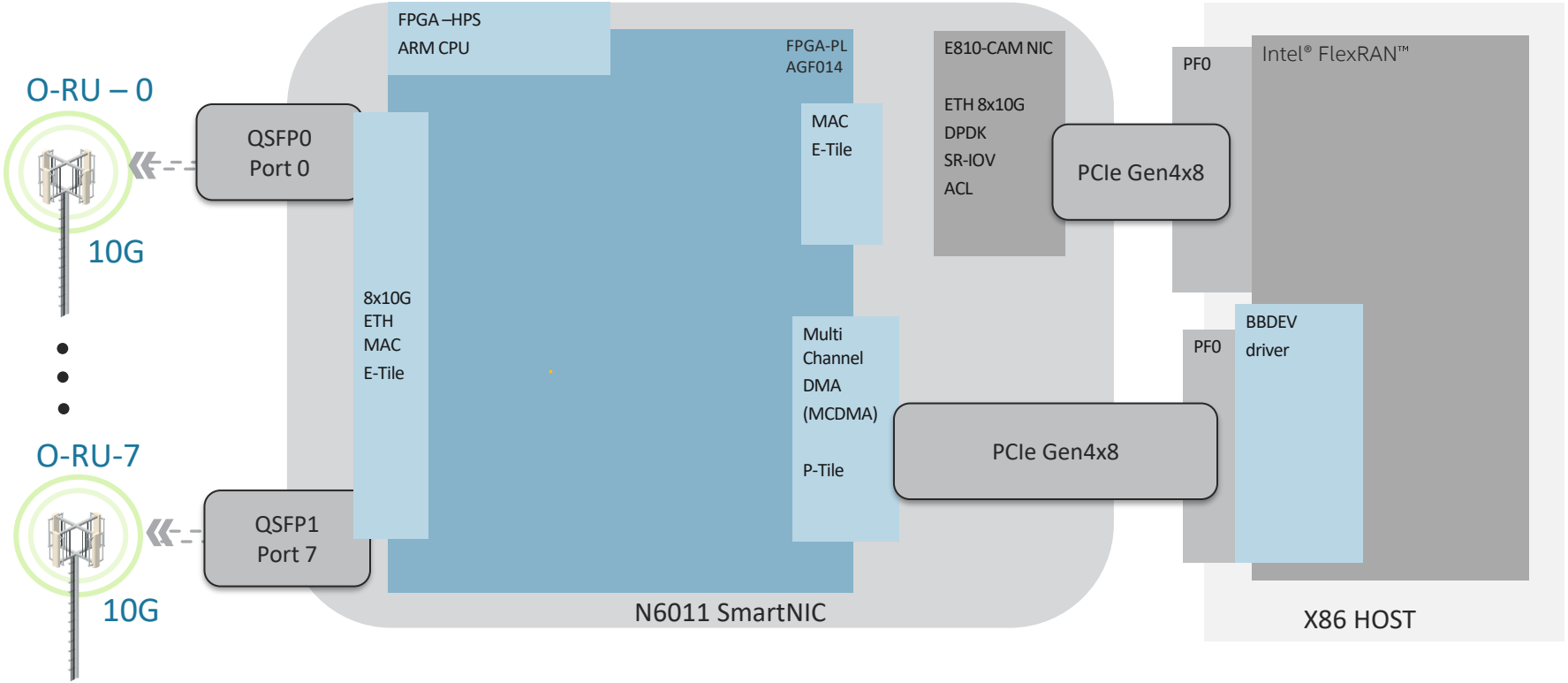
5G HW acceleration – L1 SD-FEC Use Case



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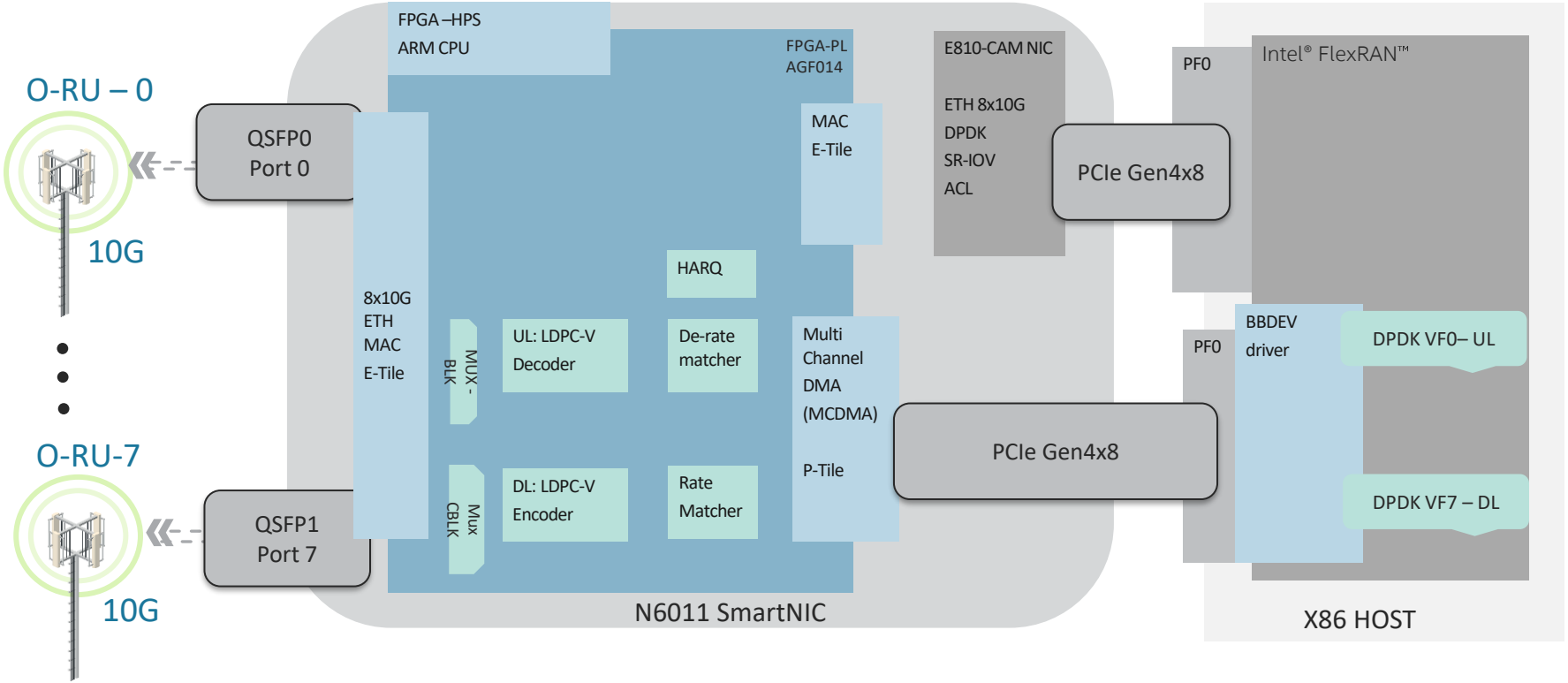
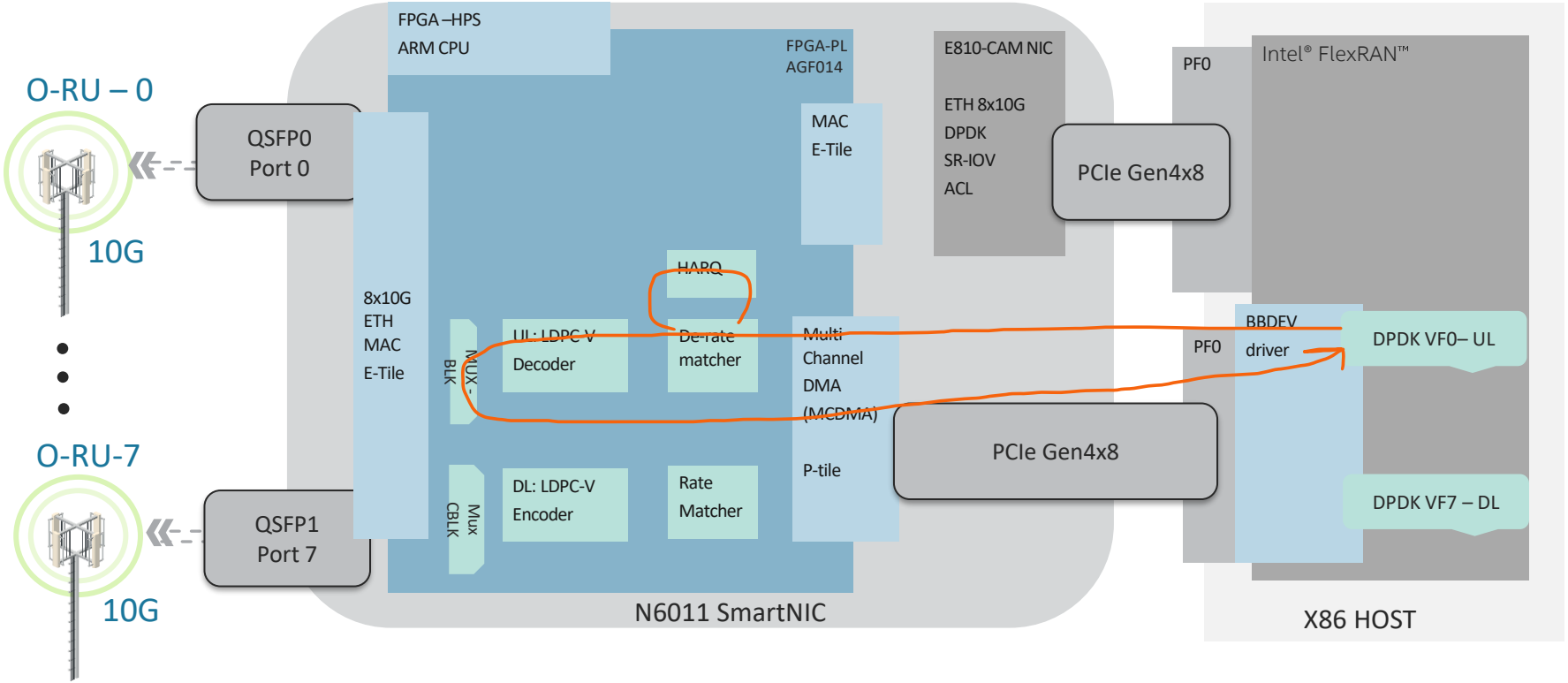
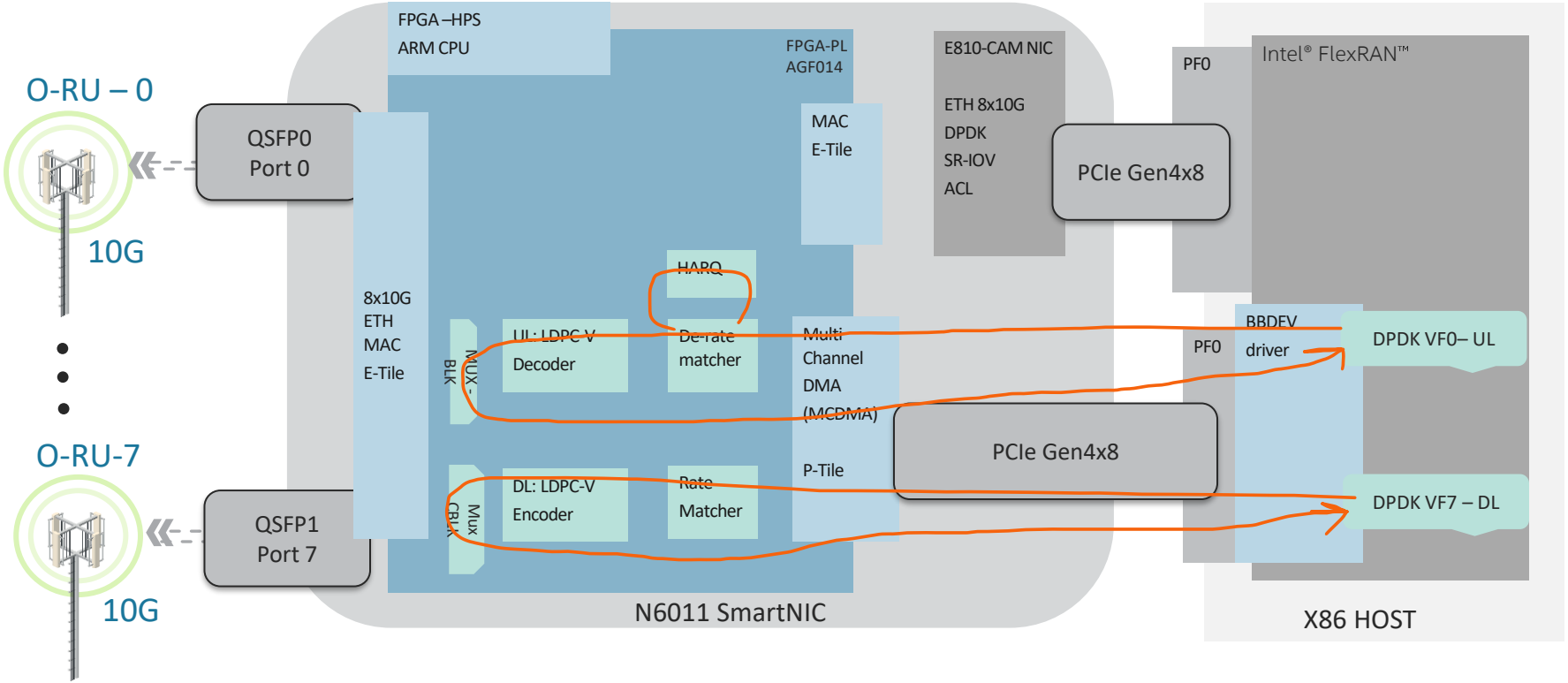
5G HW acceleration – L1 SD-FEC Use Case



5G HW acceleration – L1 SD-FEC Use Case



5G HW acceleration – L1 SD-FEC Use Case



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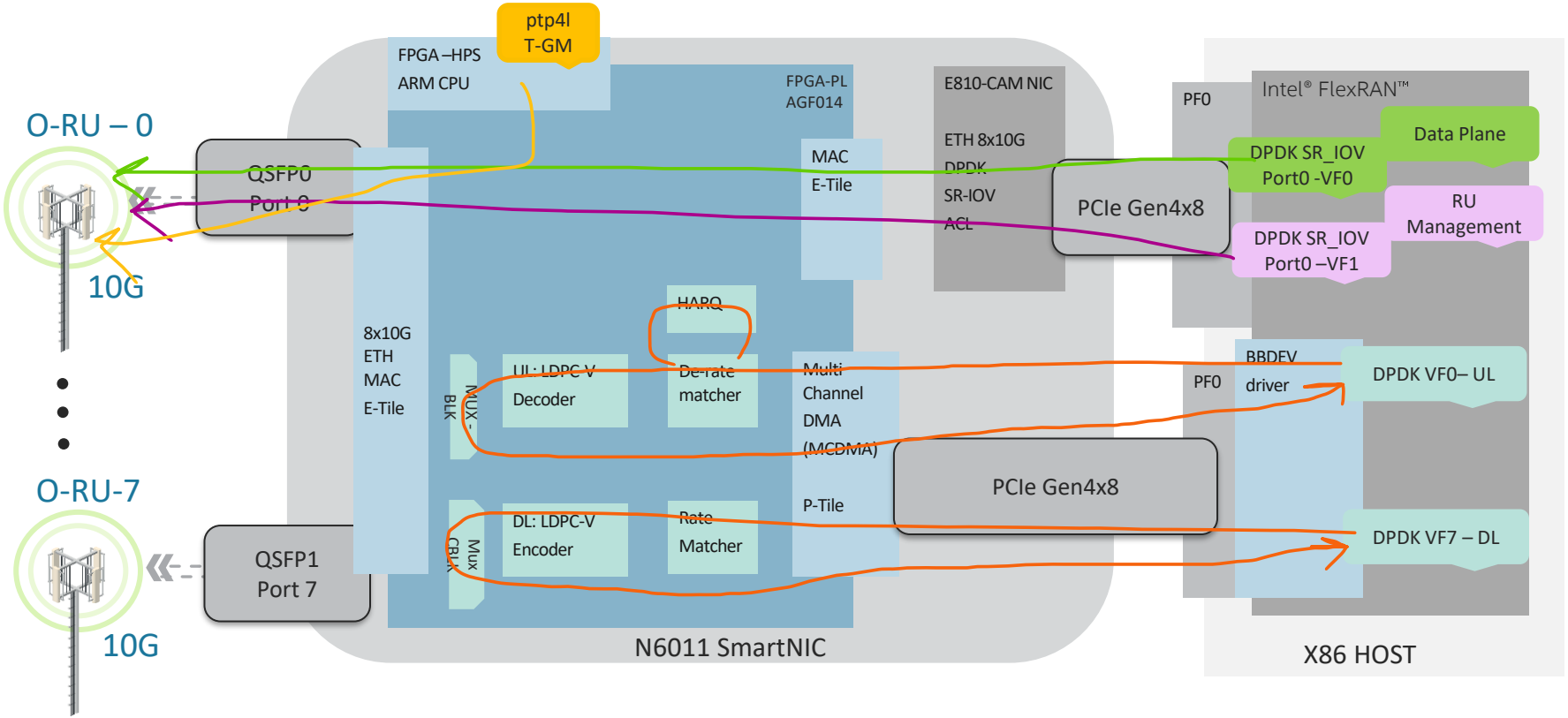
5G HW acceleration – L1 SD-FEC Use Case, vRAN workload



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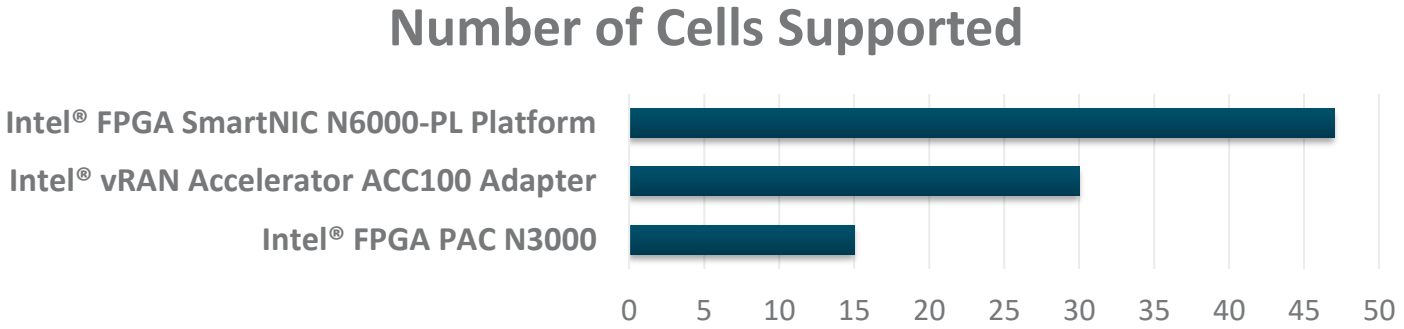
5G HW acceleration – L1 SD-FEC Use Case – vRAN workload

- Look-aside LDPC offload, compliant to 3GPP specification TS 38.214
- DPDK BBDEV Driver for Intel® FlexRAN™ from FlexRAN 22.07 version
- Support code block, transport block and code block groups acceleration
- Support HARQ, and up to 16G bytes of DDR4 for HARQ buffer
- PCIe Gen4x8 interface with 8VF/PF with multi-queue support
  - Max 32 queues for Uplink, and max 32 queues for Downlink
  - Flexible queue to VF mapping
- 2 LDPC-V decoder @467MHz, 2 LDPC-V encoder @600MHz

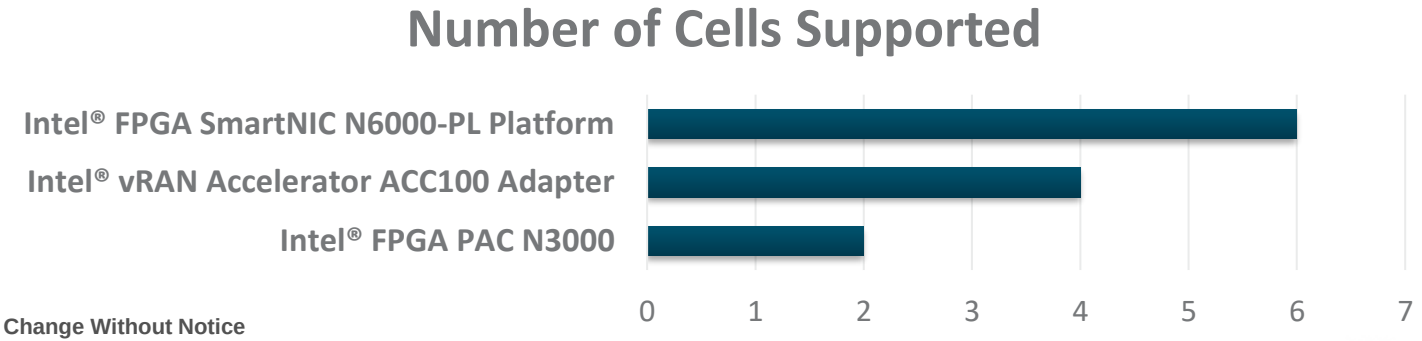
5G HW acceleration – vRAN workload performance

20MHz 4DL2UL *



** Performance varies depending on traffic model definition.*

80MHz 16DL8UL*



5G HW acceleration – vRAN workload power utilization

Component	Typ Power (W)*
AGF014 FPGA	55
DDR4 x 3 banks	3.4
E810-CAM2	13
BMC	0.6
QSFP Transcievers	6.5
PLL+OCXO	4
Supply Power Loss	10
Total	92,5

Preliminary Info – Subject to Change Without Notice

** Performance varies depending on traffic model definition.*

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5G HW acceleration – LDPC only power utilization

Component	Typ Power (W)*
AGF014 FPGA	*55*
DDR4 x 3 banks	3.4
BMC	0.6
Supply Power Loss	*10*
Total	60-69

AGF014 FPGA LDPC performance per watt (Gbps/W)*

20MHz	Peak		Average	
Cells	UL	DL	UL	DL
9 cells	0.115	0.227	0.068	0.277
18 cells	0.115	0.228	0.075	0.288

Preliminary Info – Subject to Change Without Notice

** Performance varies depending on traffic model definition.*

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N6011 SmartNIC – What's in the box?

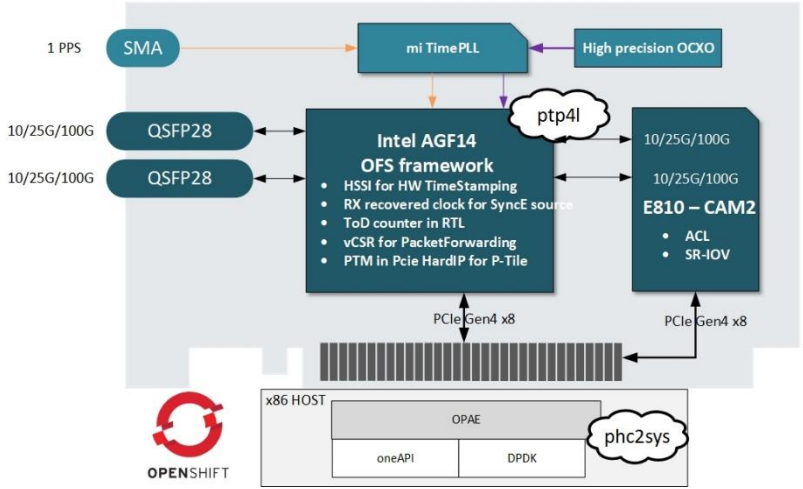
STATUS: PRODUCTION

HW

- Intel® Agilex™ 7 FPGA F-Series 014 and Intel® Ethernet Controller E810-CAM2
- Full Height ½ Length PCIe card, Single Slot
- PCIe Gen4 with 2x8 bifurcation, 2xQSFP28 Front ports
- 16GB DDR4 memory
- Optimized for 100W TDP

FPGA - FW

- Open FPGA Stack – OFS
- vRAN workload for xHAUL and LDPC acceleration
  - OFS based
  - IEEE 1588-2019 compliance for T-GM, T-BC, and SyncE
  - xHAUL features through E810 CAM and vCSR IP (with P
  - SD-FEC offload with LDPC-V encoder and decoder RTL



HOST - SW

- Up streamed Linux drivers, OPAE libraries for OFS
- DPDK with SR-IOV and Mailbox support in x86 HOST through I
- BBDev driver for Intel® FlexRAN™
- Variety of PTP stacks running on the cards SoC ARM CPU
- Openshift support for out-off-tree DFL drivers, and KMM

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N6011 SmartNIC – 5G HW acceleration benefits

STATUS: PRODUCTION

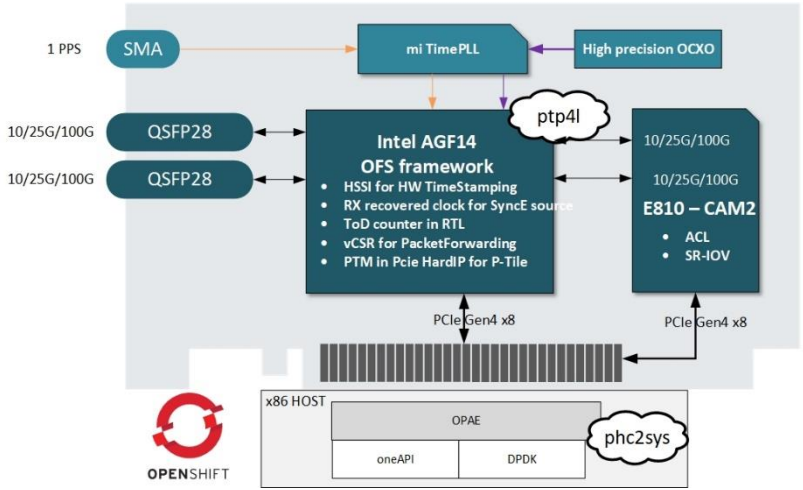
Power

- Buy less or cheaper servers (lower CAPEX)
- Reduce power consumption (lower OPEX)

Reconfigurable

- Functions can be changed as O-RAN evolves
- Add custom logic – differentiate- Multi-purpose
- Add network security features, encryption/decryp
- Improve QoS with options for deep packet inspec
- Better “EOL” support

- +1 Plug&Play replacement for any E810 based NI



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LDPC only HW acceleration – Look-a-side card

codename: ***BlueFjord***

STATUS: DEVELOPMENT

HW

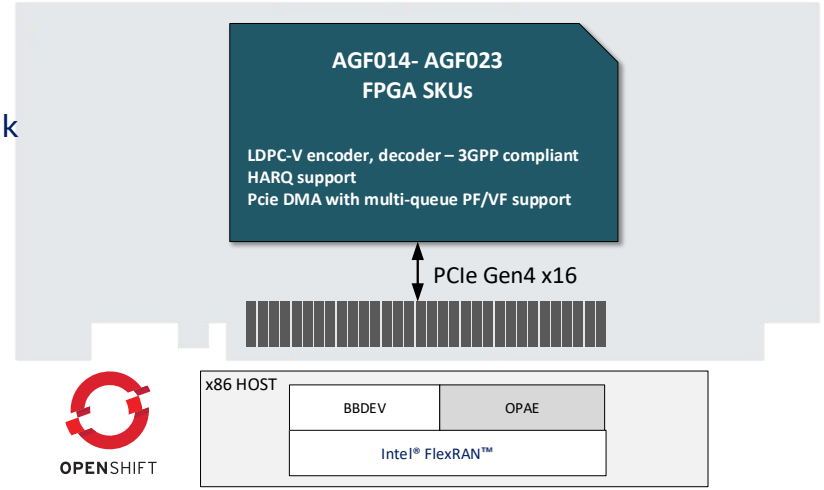
- Intel® Agilex™ 7 FPGA F-Series 014 or 023 FPGA SKUs
- ½ Height ½ Length PCIe card, Single Slot, low profile
- PCIe Gen4 x16 Host Interface
- 2x72-bit DDR4 interfaces with 4GB component memory/bank
- Optimized for <75W TDP

FPGA - FW

- vRAN workload for LDPC acceleration
  - SD-FEC offload with LDPC-V encoder and decoder RTL IPs

HOST - SW

- Up streamed Linux drivers, OPAE for card management
- BBDev driver for Intel® FlexRAN™
- Openshift support for out-off-tree DFL drivers, and KMM



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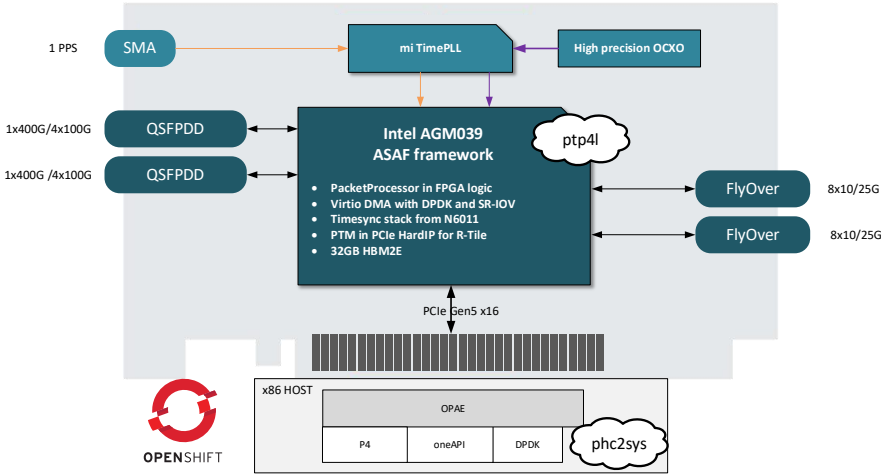
400G Ethernet HBM SmartNIC

codename: ***ThunderFjord***

STATUS: PROTOTYPE

HW

- Intel® Agilex™ 7 FPGA M-Series (AGM039) with 32GB HBM2e
- Full Height, 3/4 Length, Dual Slot
- 2xQSFPDD56 for 2x400G or 2x4x100G Ethernet
- High Speed(HS)Connector with FireFly edge card for:
  - 16x10/25G or 4x100G Ethernet or
  - PCIe Gen4x16
- PCIe Gen5 x16 with PTM and CXL support
- Optimized for 225W-250W TDP



FPGA FW

- Application Stack Acceleration Framework(ASAF)
- PacketProcessor with match/action routing
- Virtio DMA with DPDK support

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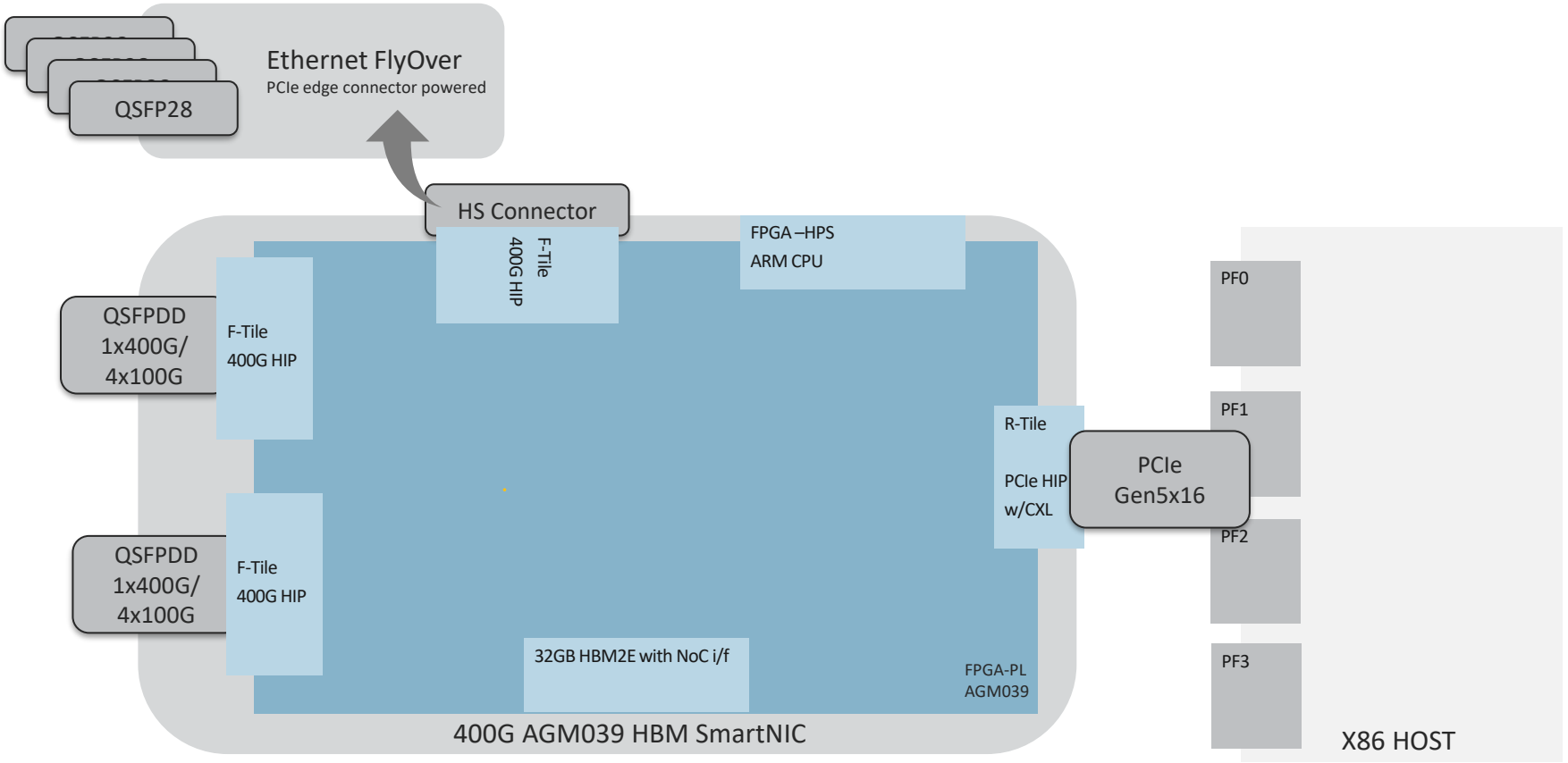
400G Ethernet SmartNIC – 5G Core, UPF, FHGW



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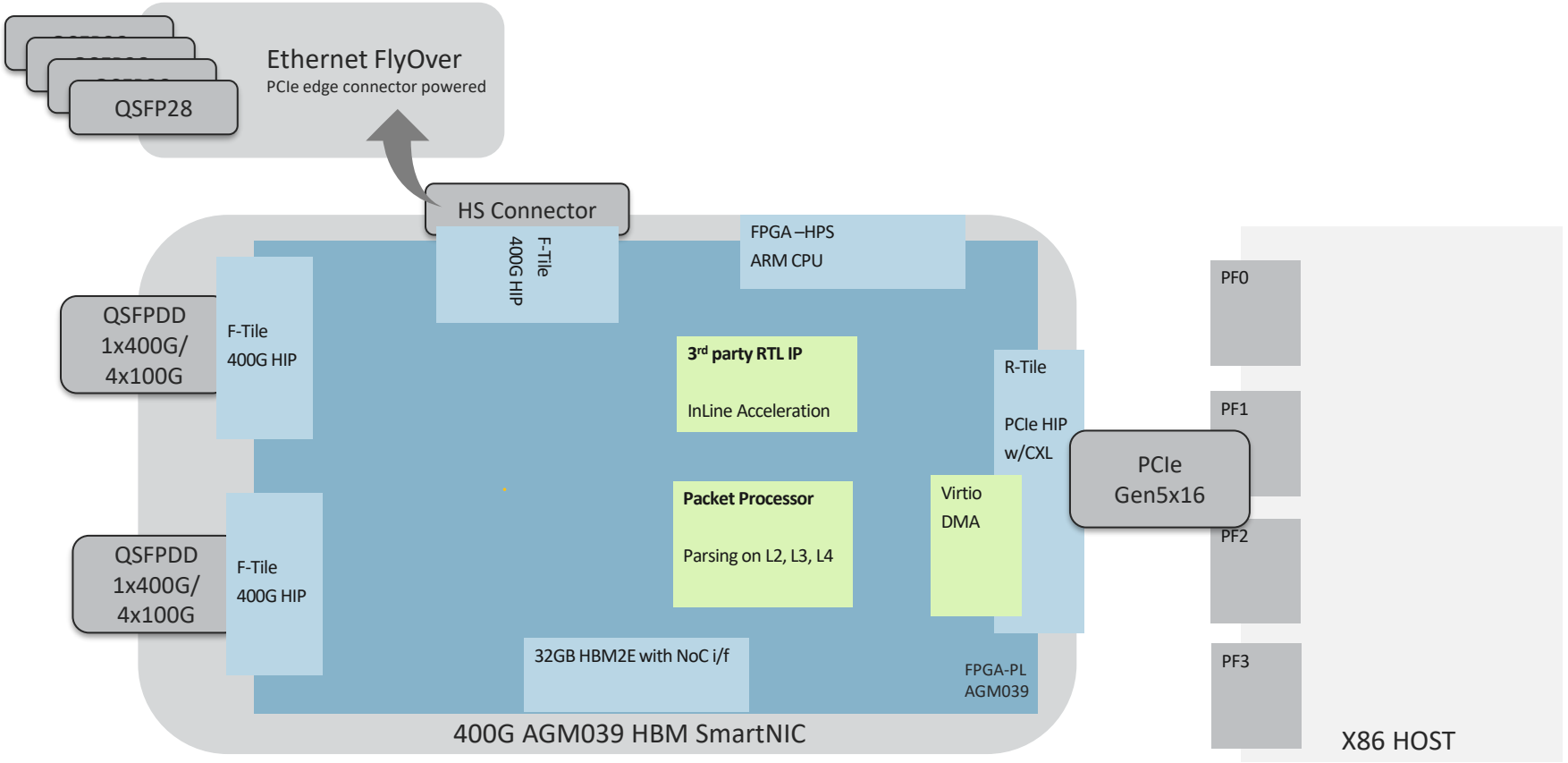
400G Ethernet SmartNIC – 5G Core, UPF, FHGW



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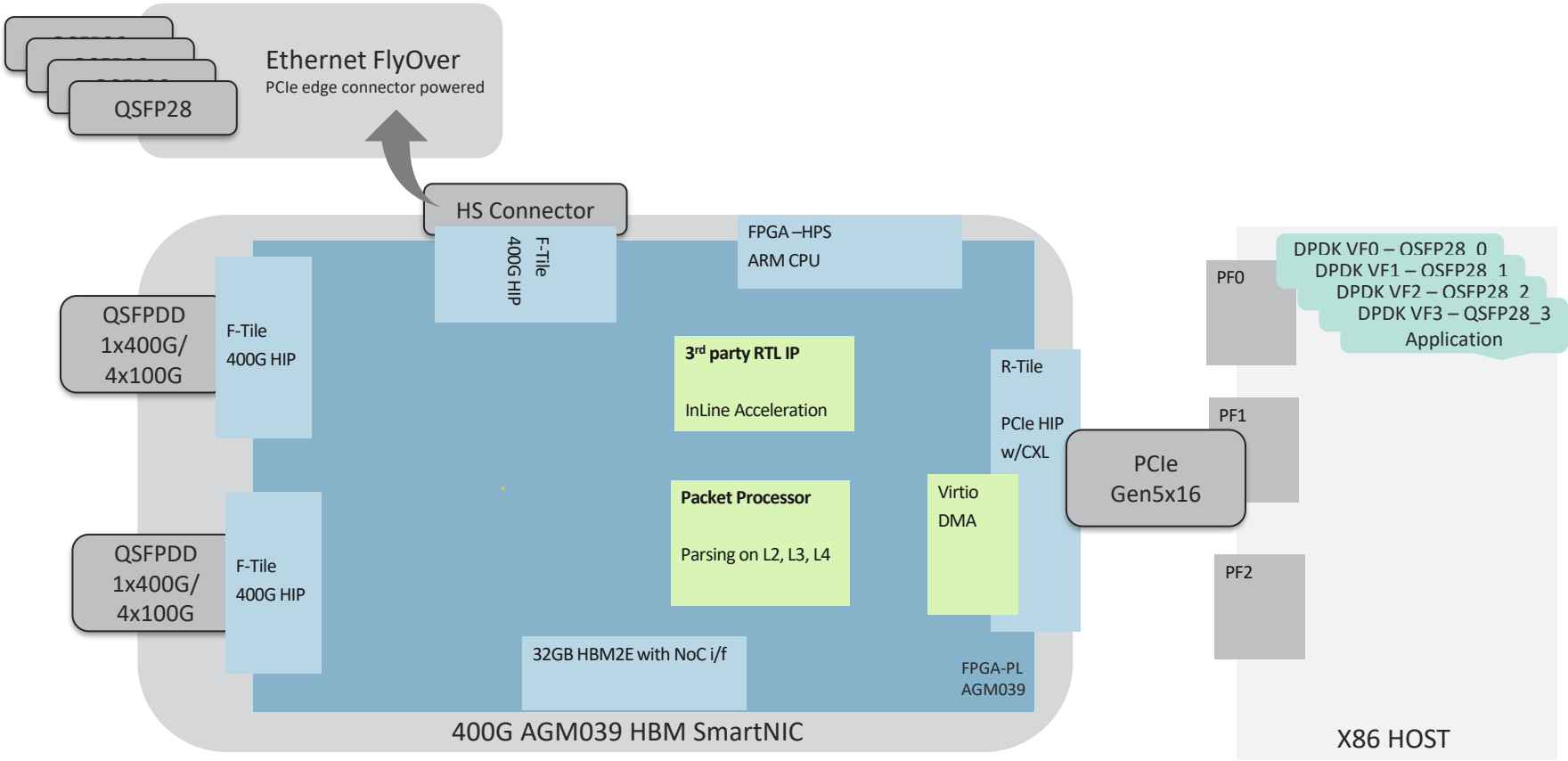
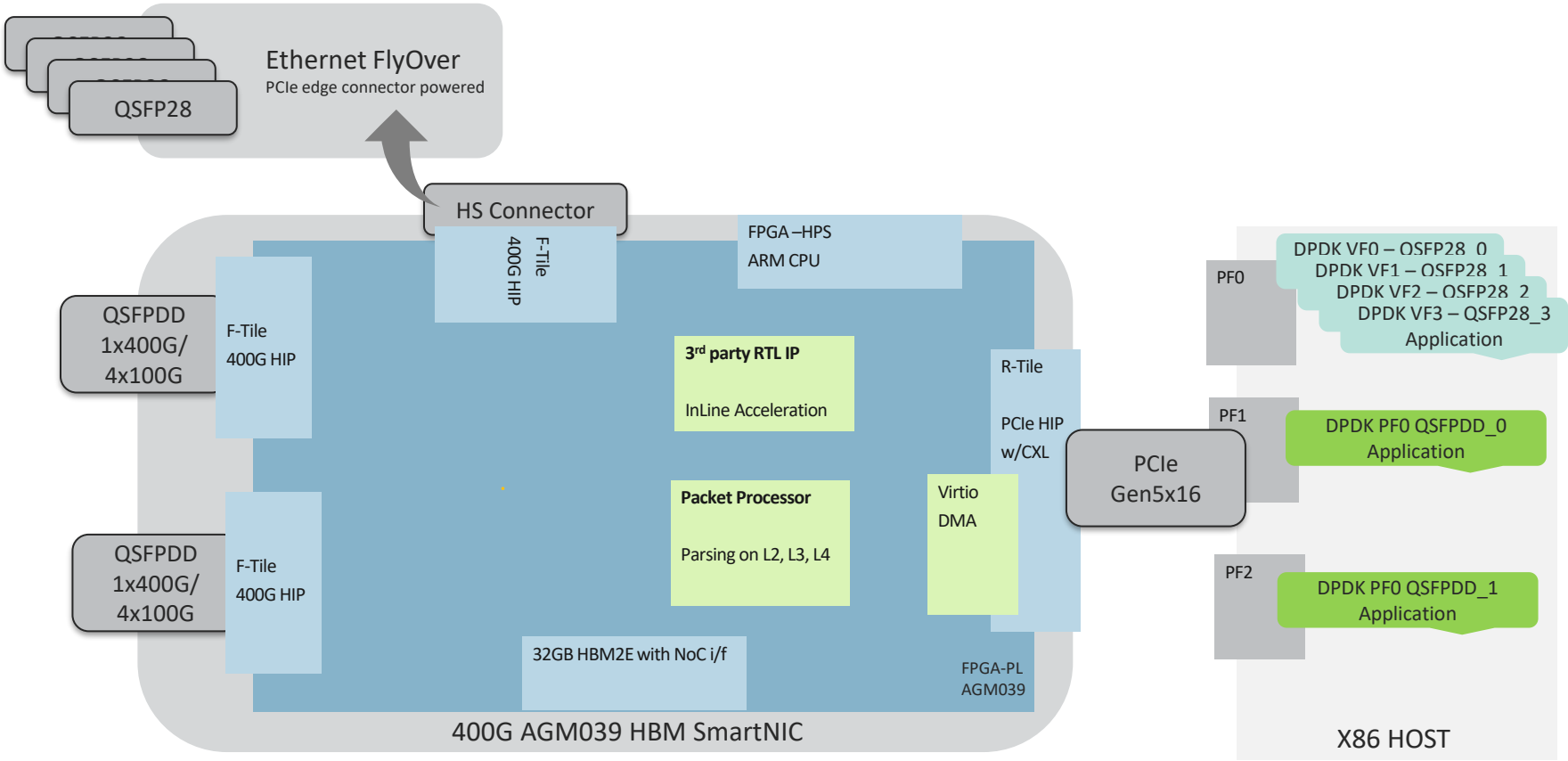


400G Ethernet SmartNIC – 5G Core, UPF, FHGW



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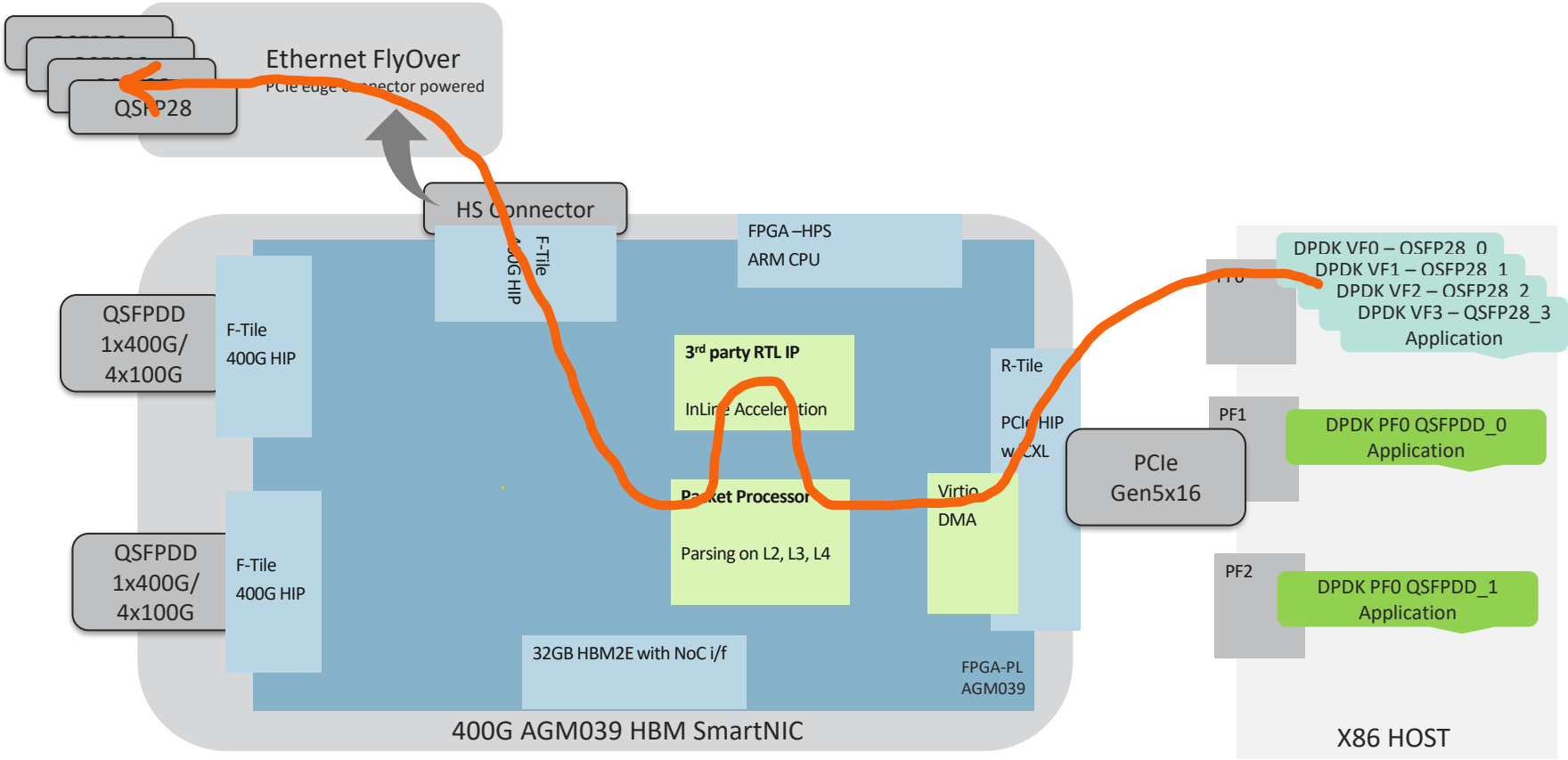
400G Ethernet SmartNIC – 5G Core, UPF, FHGW



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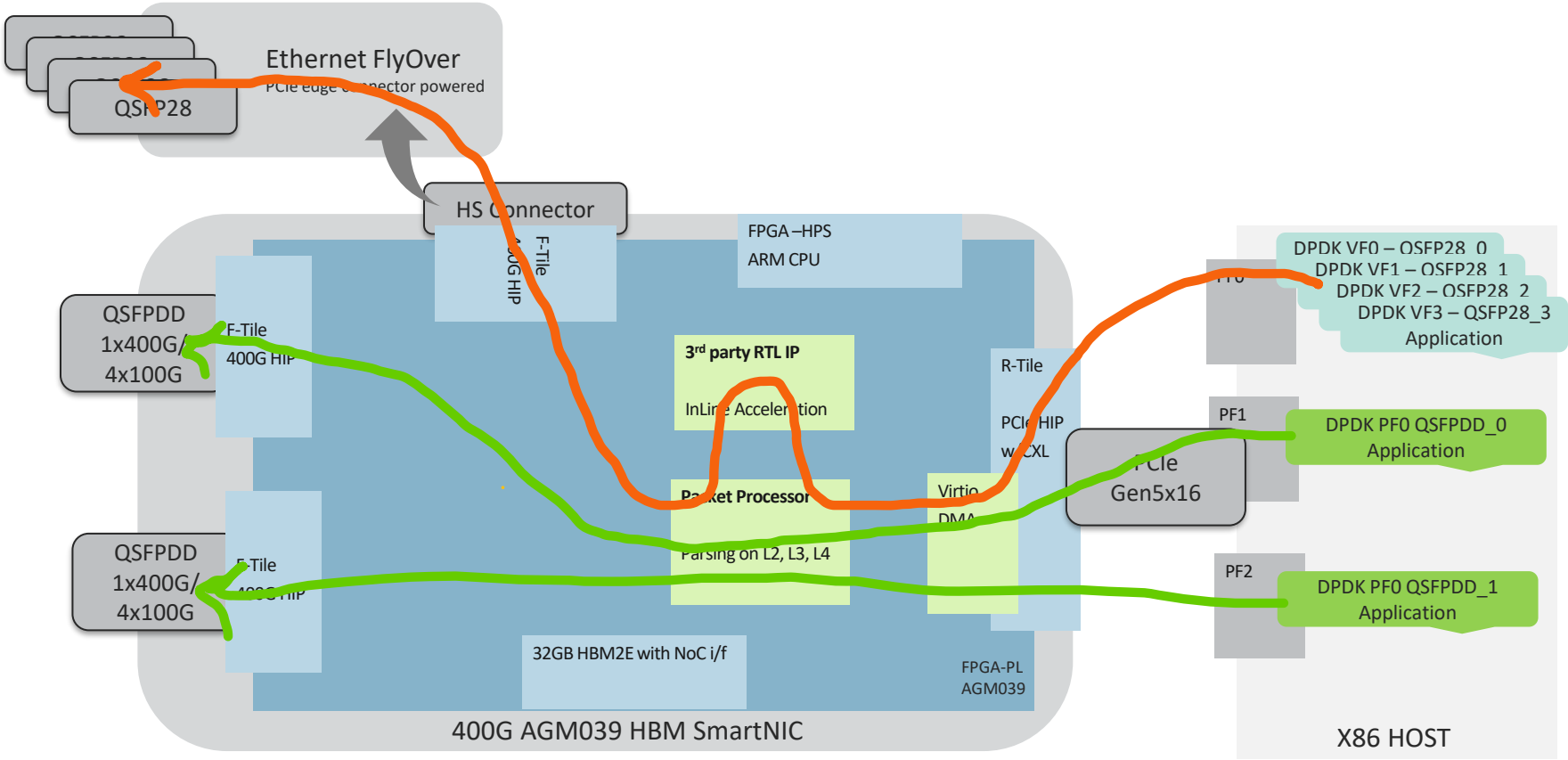

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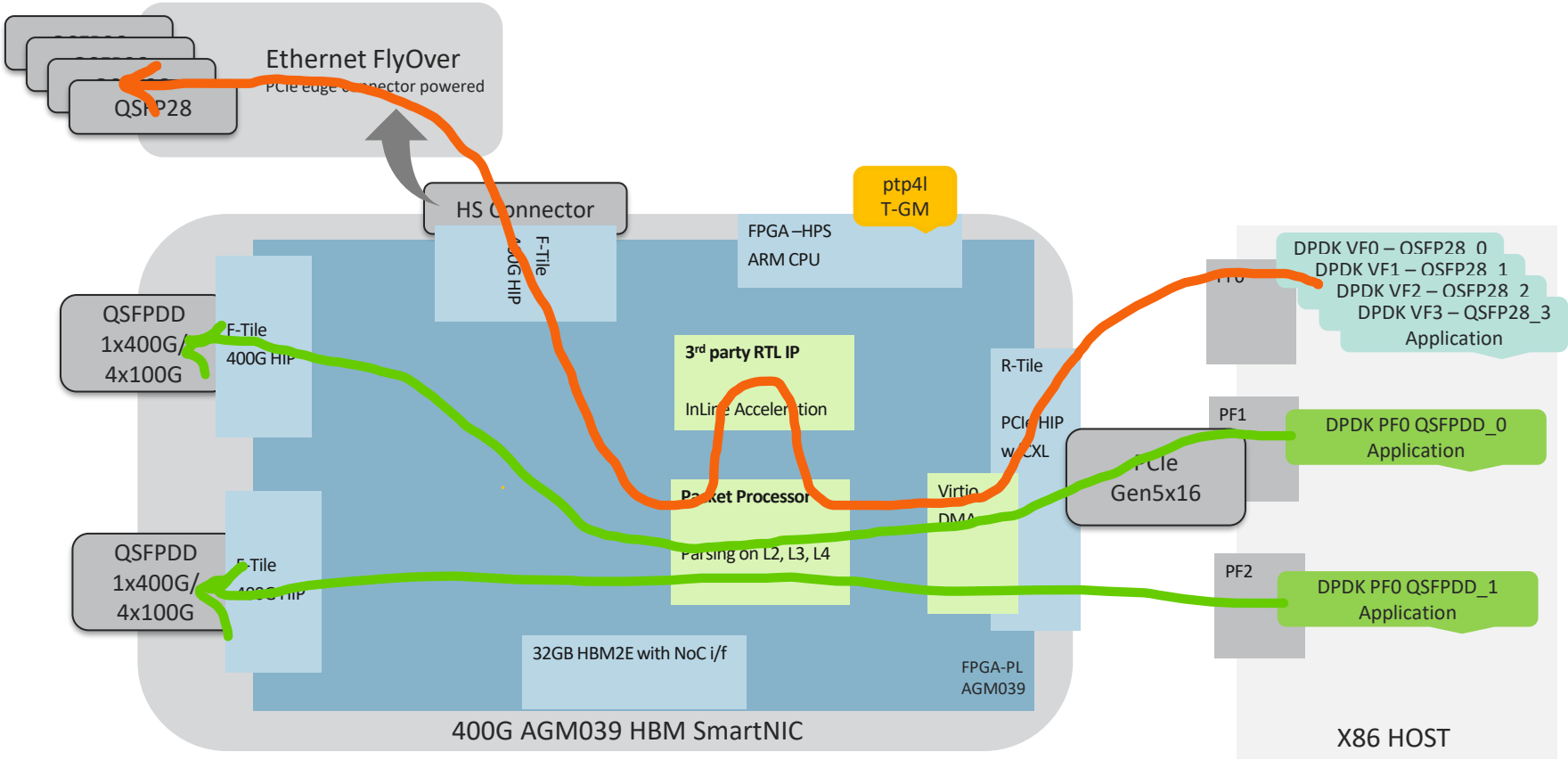

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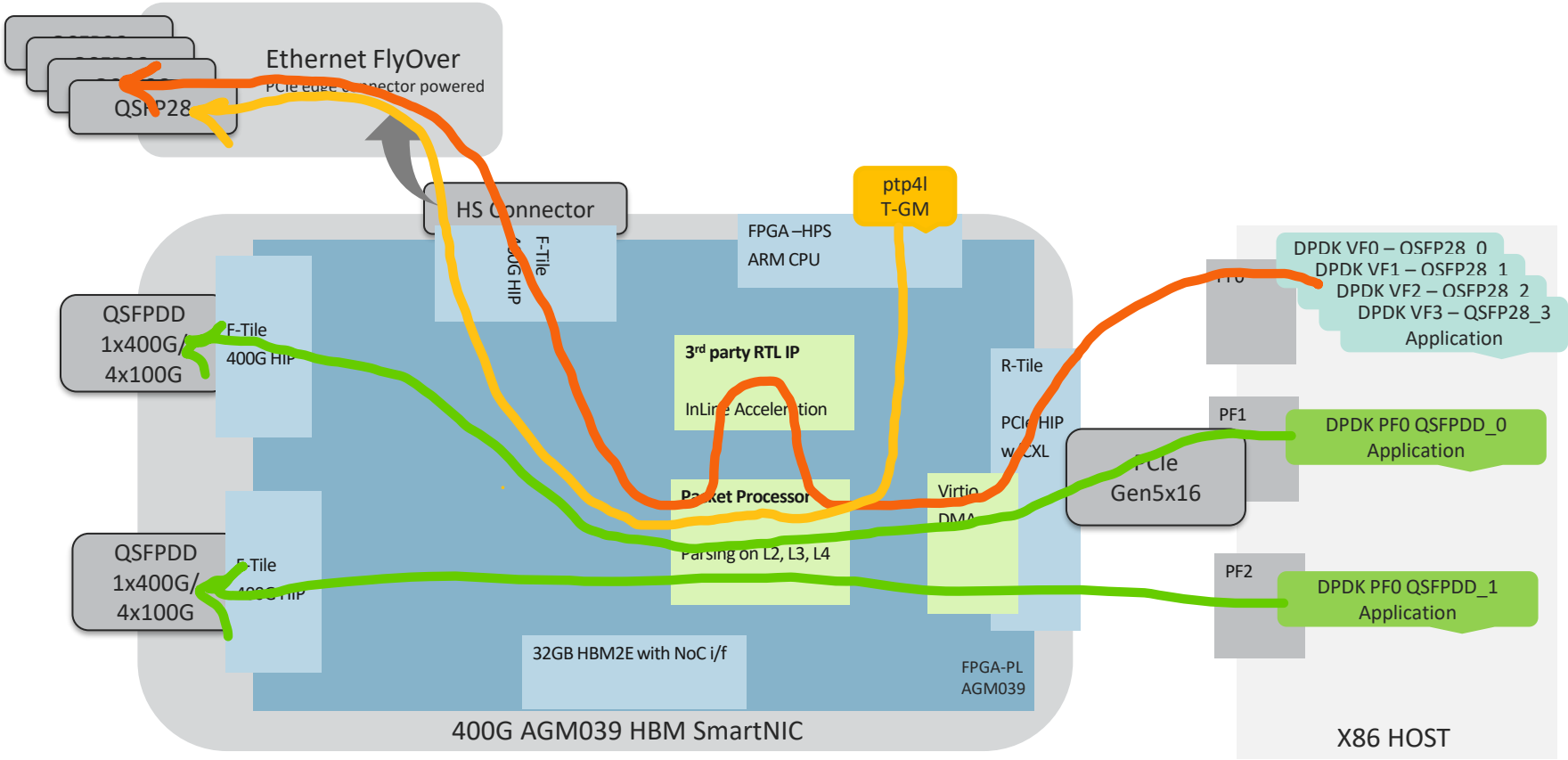

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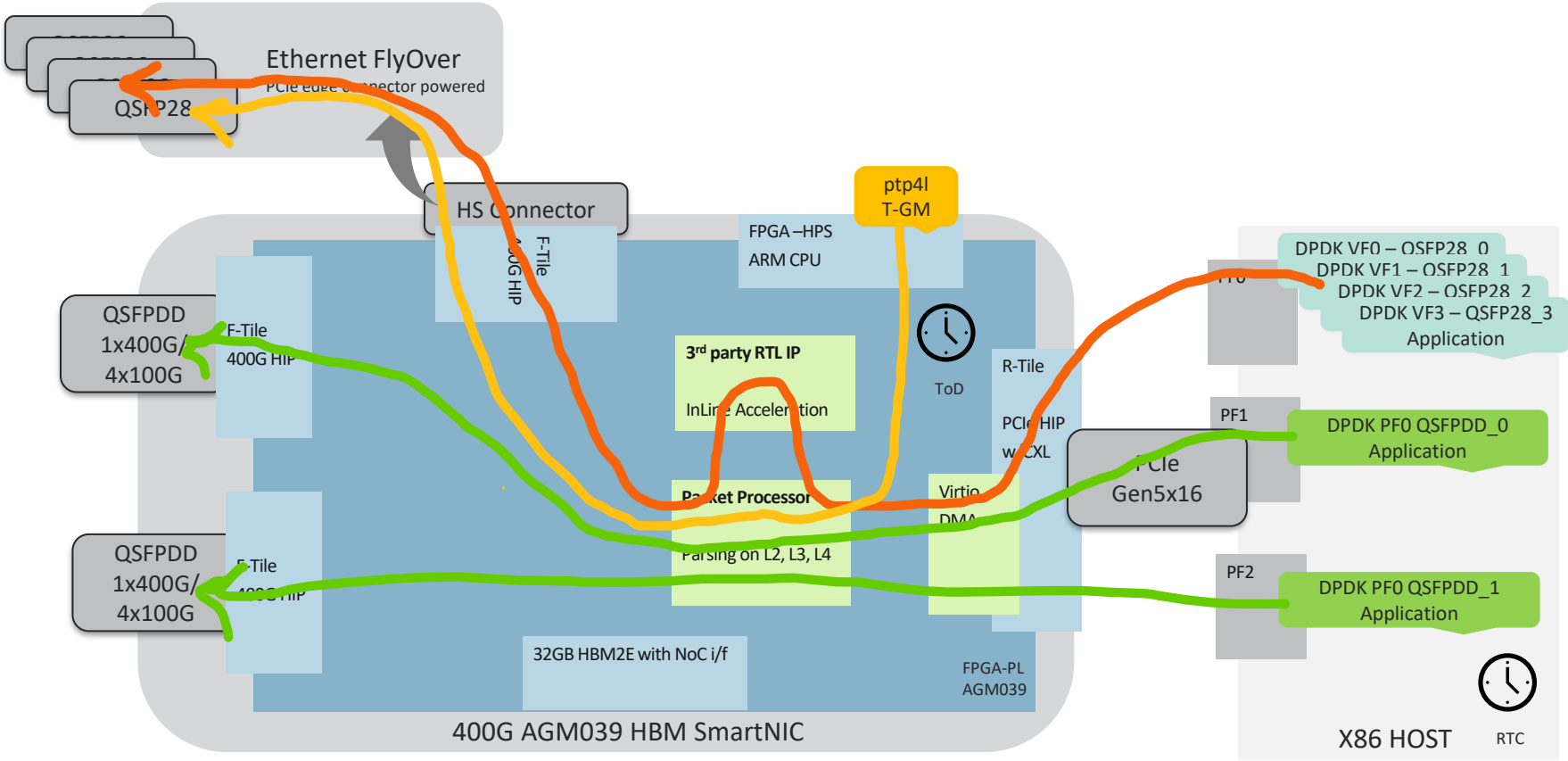

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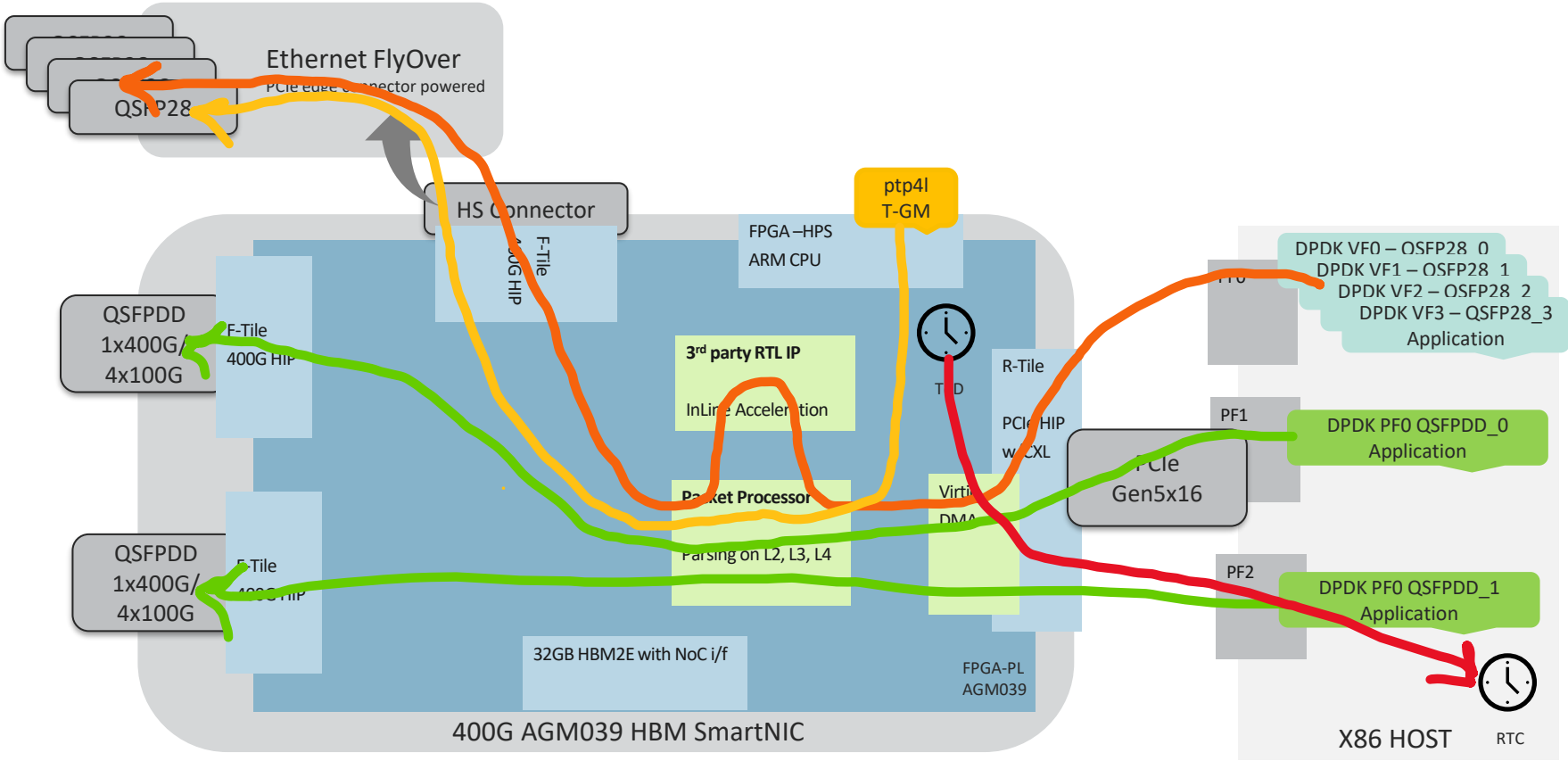

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Thank You!

For more info visit:

www.silicom.dk

Date: May 14, 2024
Time: 9AM PDT / 12PM EDT

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